5-2013

LC oscillator chirp generator for LADAR applications

Joseph Richard Grace III

LC OSCILLATOR CHIRP GENERATOR

FOR LADAR APPLICATIONS

By

Joseph Richard Grace III

B.S. University of Maine, 2011

A THESIS

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

(in Electrical Engineering)

The Graduate School

The University of Maine

May 2013

Advisory Committee:

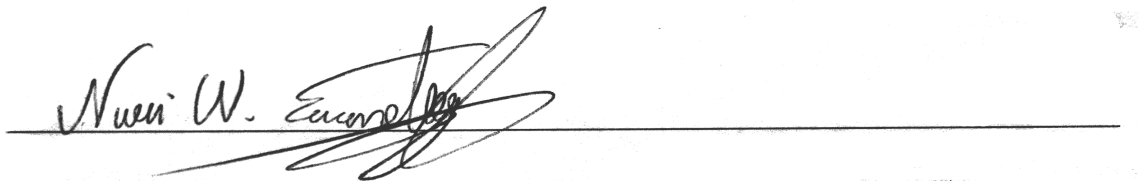
Nuri W. Emanetoglu, Assistant Professor of Electrical and Computer Engineering, Advisor

Donald M. Hummels, Professor and Chair of Electrical and Computer Engineering

David E. Kotecki, Associate Professor of Electrical and Computer Engineering

THESIS ACCEPTANCE STATEMENT

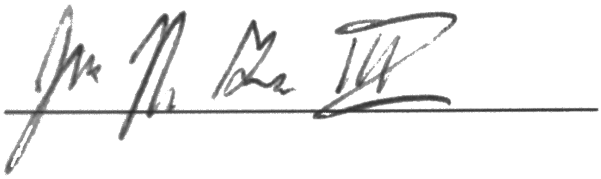
On behalf of the Graduate Committee for Joseph Richard Grace III, I affirm that this manuscript is the final and accepted thesis. Signatures of all committee members are on file with the Graduate School at the University of Maine, 42 Stodder Hall, Orono, Maine.



Dr. Nuri Emanetoglu, Assistant Professor of Electrical and Computer Engineering April 19th, 2013

LIBRARY RIGHTS STATEMENT

In presenting this thesis in partial fulfillment of the requirements for an advanced degree at The University of Maine, I agree that the Library shall make it freely available for inspection. I further agree that permission for "fair use" copying of this thesis for scholarly purposes may be granted by the Librarian. It is understood that any copying or publication of this thesis for financial gain shall not be allowed without my written permission.

Signature:  Date: 5/1/2013

Joseph R. Grace III

LC OSCILLATOR CHIRP GENERATOR

FOR LADAR APPLICATIONS

By Joseph R. Grace III

Thesis Advisor: Dr. Nuri Emanetoglu

An Abstract of the Thesis Presented
in Partial Fulfillment of the Requirements for the
Degree of Master of Science
(in Electrical Engineering)
May 2013

The design, layout, simulation, and testing of a signal generator integrated circuit (IC) intended to create a frequency modulated chirp signal used in Laser Assisted Detection and Ranging (LADAR) systems are described. LADAR systems function by illuminating a target with a laser beam and measuring the properties of the reflected signal. Applications include range finding, collision avoidance, terrain mapping, and facial recognition. The development and improvement of LADAR IC design can lead to miniaturized LADAR-on-chip systems that could significantly improve the usability and applications of said systems. Two designs, a fixed frequency oscillator bank (FFOB) and a voltage controlled oscillator bank (VCOB), were investigated as signal generators for chirped LADAR systems. The FFOB was designed to operate at 16 discrete frequencies ranging from 600 MHz to 2.1 GHz. The VCOB design offers a continuously variable frequency output ranging from 1 GHz to 3 GHz and outputs 32 discrete frequencies ranging from 1.5 GHz to 3.05 GHz in the suggested configuration. The

FFOB design consists of 16 individual oscillators that are each controlled by a logical input pin on the package. In contrast, the VCOB design consists of eight oscillators, each with a tunable frequency and are cycled automatically by an on-chip digital counter circuit. All designs were completed in the IBM CMRF7SF process. The FFOB IC design was manufactured and packaged by MOSIS, and testing of the FFOB chip was completed. The VCOB IC was was designed to improve the performance of the FFOB signal generator by lowering power consumption, reducing signal distortion, increasing the number of the steps in the chirped waveform, and increasing bandwidth.

DEDICATION

For my loving mother

ACKNOWLEDGMENTS

There are many people that have contributed to both this work and to my graduate education as a whole. Without them, this would not have been possible. My special thanks to:

Nuri Emanetoglu

David Kotecki

Donald Hummels

Eric Beenfeldt

Duane Hanselman

John Vetelino

Andrew Sheaff

Mauricio Pereira da Cunha

Richard Eason

Bruce Segee

Alex Bryant

Derrill Vezina

Khayyam Mohammed

Fred Graunke

Steven Swan

Keith Scidmore

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF ACRONYMS

IC	Integrated Circuit
RF	Radio Frequency
FM	Frequency Modulation
AM	Amplitude Modulation
LADAR	Laser Assisted Detection and Ranging
RADAR	Radio Assisted Detection and Ranging
MOSIS	Metal Oxide Semiconductor Implementation Service
OEM	Optoelectronic Mixer
TZA	Transimpedance Amplifier
LO	Local Oscillator
IF	Intermediate Frequency
FFT	Fast Fourier Transform
DSP	Digital Signal Processing
FM CW	Frequency Modulated Continuous Wave
ARL	Army Research Laboratory
VCO	Voltage Controlled Oscillator
PLL	Phase Locked Loop
ESD	Electrostatic Discharge
HBM	Human Body Model
CDM	Charged Device Model

LIST OF ACRONYMS

DIP	Dual In-line Package
I/O	Input/Output
FFOB	Fixed Frequency Oscillator Bank
VCOB	Voltage Controlled Oscillator Bank

Chapter 1

INTRODUCTION

1.1 Motivation

Laser Assisted Detection and Ranging (LADAR) is a sensing technology that may be used to gather information about a target including distance, velocity, and other metrics. The fundamentals of LADAR involve using a specific signal to drive a laser or array of lasers and illuminate a target. A reflected light signal is sensed by the LADAR device, and the desired information is extrapolated. LADAR is commonly compared to radar, the radio wave analog to LADAR.

LADAR is a desirable technology for a number of reasons. The frequency of the light used in LADAR systems can be in the ultraviolet, visible, and near infrared range of the spectrum, and thus has a comparatively smaller wavelength than its radio counterpart in radar. This allows LADAR to have a better performance in sensing very small objects. In addition to this improved resolution, LADAR also benefits from the inherent advantages of lasers— excellent beam density and coherence [1]. This allows for the technology to be used to sense and build three dimensional images with relative precision compared to radar. LADAR is useful in the detection of sea-skimming cruise missiles, where scattering from the sea surface presents problems for radar due to the small beamwidth of LADAR [1]. This also makes LADAR less detectable by enemy combatants [2]. LADAR also allows for the generation of 3D images that are valuable in target identification and clutter penetration via the use of focal plane resolution [3].

1.2 Scope of Work

Typical LADAR systems consist of a number of circuit components including signal generators and oscillators, direct digital synthesizers (DDS), radio frequency (RF) amplifiers, optoelectronic mixers (OEMs), photodetectors, and of course, lasers. This work describes the design, layout and testing of a circuit to be used as a signal generator that may drive both the sending laser and the receiving photodetector mixer blocks of a compatible LADAR system. The details explaining the circuit blocks mentioned here are found in Chapter 2.

This work includes two different designs, a fixed frequency oscillator bank (FFOB) and a voltage controlled oscillator bank (VCOB) design. The first utilizes a switched set of sixteen fixed frequency LC oscillators that are intended to function as the signal generator block necessary to drive a laser with a "chirp" signal. A detailed explanation of this chirp signal is found in Chapter 2. The chirp signal created by this design ranges from 600 MHz to 2.1 GHz at sixteen discrete intervals spaced 100 MHz apart. This chip was designed and laid out in the Cadence design environment and manufactured by the MOSIS. IC testing and characterization was then completed on the FFOB, which lead to the design and layout of a new, more robust and flexible iteration, the VCOB.

The second design, the VCOB, features eight voltage controlled oscillators but operates over a slightly wider bandwidth. In this design, the chip generates 32 discrete frequencies ranging from 1.5 GHz to 3.05 GHz, twice the number of points as the first chip. Additionally, the VCOB has a built-in digital counter circuit used to switch between each of the operating frequencies without the need for additional off-chip control circuitry.

Each oscillator in the VCOB may also be adjusted in frequency in a custom configuration with an off-chip bias voltage for more flexible frequency adjustments. A number of small improvements were also made to make the circuit operate more reliably and increase its frequency tunability as well. This second chip has been designed and laid out and is ready for manufacture and packaging.

1.3 Organization of Thesis

This thesis is comprised of five chapters. Chapter 1 has provided a brief introduction to the motivation and the scope of the completed work. Chapter 2 describes the technical background involved, including LADAR fundamentals and the nature of the so-called chirp signal. Also covered in Chapter 2 is the circuit theory used in the design of the oscillators presented in this work. The circuit design, layout and testing of the FFOB can be found in Chapter 3, while Chapter 4 covers the VCOB. Finally, Chapter 5 is comprised of conclusions regarding the work completed and also thoughts on future work.

Chapter 2

TECHNICAL BACKGROUND

2.1 Chapter 2 Introduction

The purpose of this chapter is to provide the background information necessary to understand LADAR systems as a whole as well as the specifics related to this project. Section 2.2 covers the basics of LADAR operation before Section 2.3 delves into the details of the various subcircuits that make up a LADAR system. The send and receive portions of the system are covered in Sections 2.3.1 and 2.3.2, respectively. Section 2.3.3 covers the chirp signal generation on which this work is focused. Finally, Section 2.4 covers the circuit theory behind the LC oscillators used in this work.

2.2 LADAR Fundamentals

The fundamental operation of LADAR systems consists of sending a laser beam to a target, receiving its reflection, and comparing the reflected signal to the transmitted signal. A chirped modulating signal is used in the LADAR system on which this work focuses. This is the signal used to bias the laser and photodetector mixer and is discussed further in section 2.4. The specifics of laser choice, beam focus, signal bandwidth, et cetera will vary based on the desired application.

A collision avoidance system meant to alert a motorist of unseen obstacles while backing up a minivan in a parking lot will have a different set of requirements than a target recognition system used inside of a projectile in a military application, for example. The following sections are meant to take a general approach to describing LADAR systems of all types.

2.3 LADAR Subcircuits

There are a number of circuit blocks that are fundamental to all chirped LADAR systems. They include, but are not limited to: local oscillators, photodiodes, lasers, RF amplifiers, fourier transform networks, and RF mixers. How these pieces can fit together is described below in Figure 2.1. The subsections to follow will offer brief descriptions of the functionality and motivation behind each of the blocks pictured below.

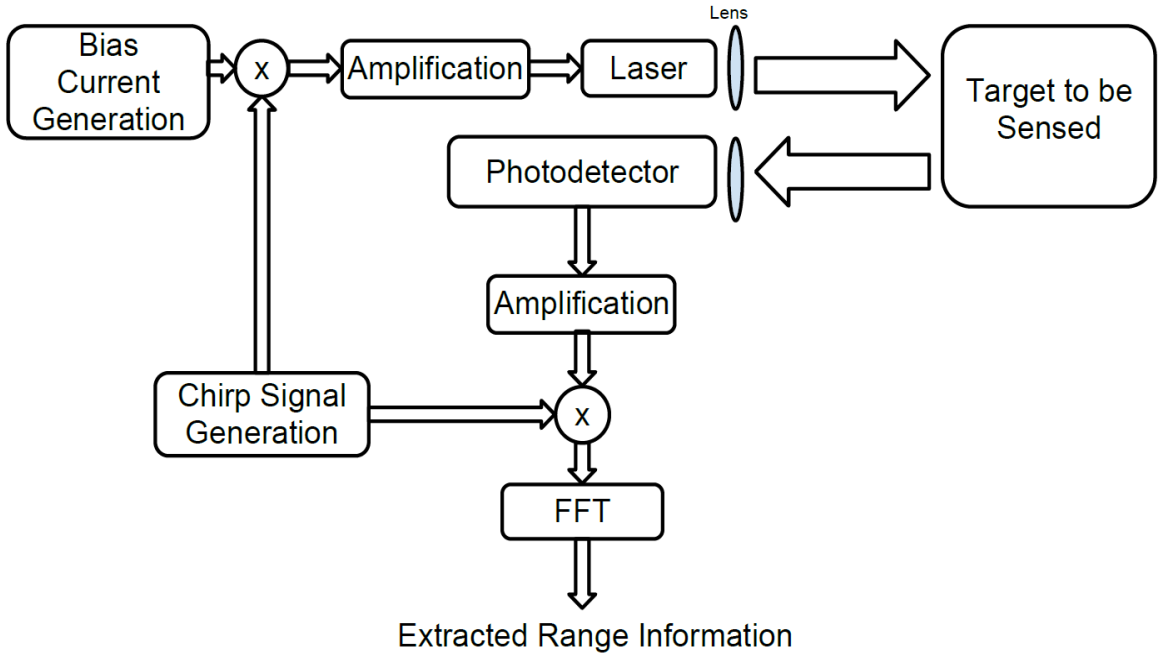


Figure 2.1: LADAR Block Diagram

2.3.1 The Laser and Biasing

Figure 2.2 below highlights the transmitter portion of the LADAR system being discussed in this subsection.

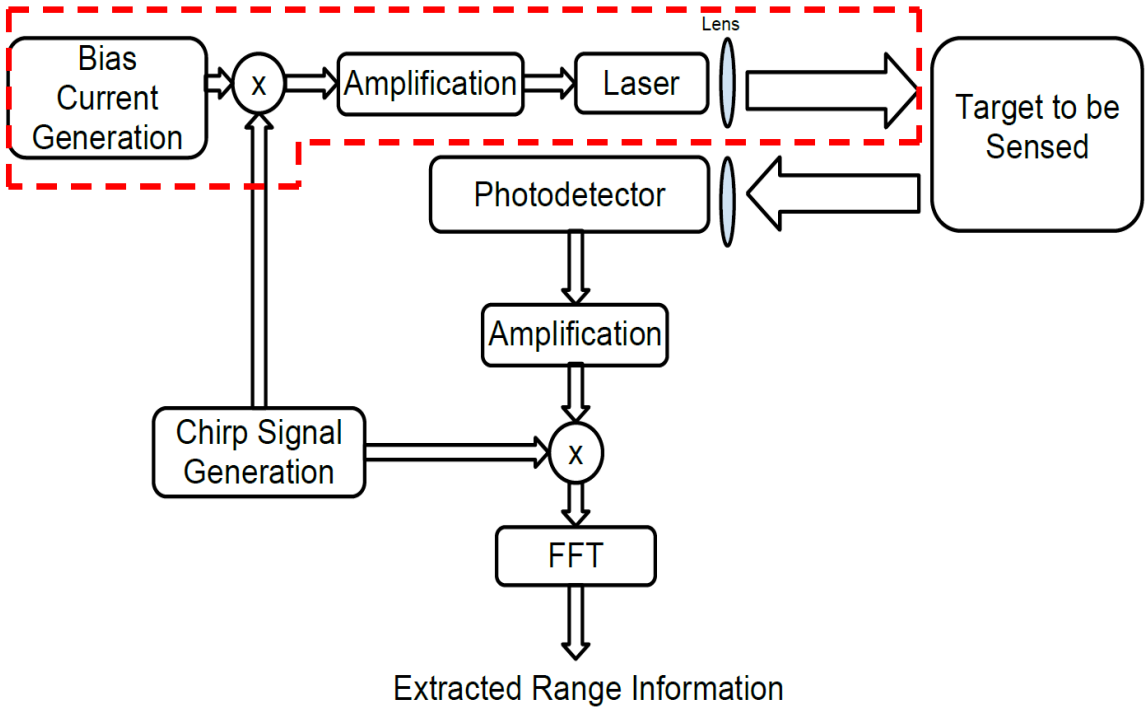


Figure 2.2: The Laser Biasing Setup

While the type of laser and biasing requirements will depend on the application, LADAR systems rely on driving the laser in the way depicted in Figure 2.2. A power source is used to generate the bias current necessary to drive the laser, which serves as the carrier signal when modulated with the output of the chirp generator. This results in the desired modulated bias current being used to drive the laser, perhaps after an amplification stage if necessary. The laser may also be fed into a collimating lens before being transmitted into free space.

2.3.2 Photodetection, Mixing, Data Extraction

Figure 2.3 below highlights the receive portion of the LADAR system being discussed in this subsection.

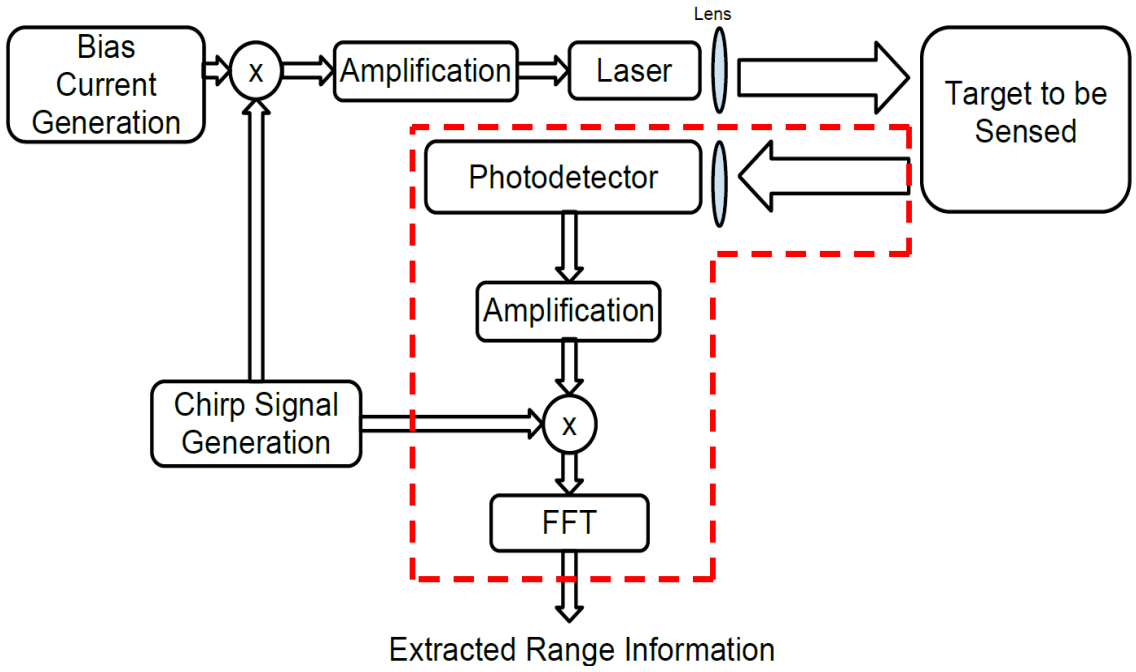


Figure 2.3: The Detection, Mixing, and Data Extraction

The light reflected off of the target may be directed through a focusing lens before being sensed by either a photodetector or photodetector array. This signal is amplified and then mixed with the original chirp signal that was used to modulate the laser. By performing this mixing, the received signal is compared to the transmitted signal, and when low pass filtered, the difference in frequency between the two signals is obtained. This provides the information necessary to extract the desired metrics about the target.

Note that the photodetection and mixing stages are sometimes combined into a single device stage known as an optoelectronic mixer (OEM)[2]. The figure below clarifies the components of the receiver in a typical LADAR system.

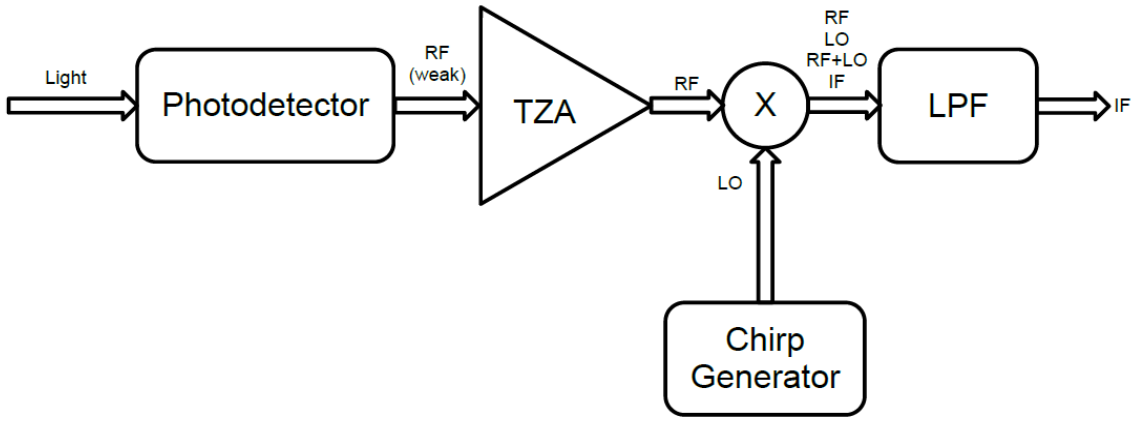


Figure 2.4: Detailed Block Diagram of Receive System [4]

As Figure 2.4, shows, the signal comes into the photodetector as light, and a weak RF signal is produced. This weak signal is then amplified by the transimpedance amplifier (TZA) stage. The chirp generator provides the local oscillator (LO) signal that is then mixed with the RF output of the TZA. Four different frequency components are output from the mixing stage: the original RF and LO signals, and signals at the sum and difference frequencies of the two inputs. The difference signal, known as the intermediate frequency (IF) signal, is the desired signal for the LADAR system. To isolate this signal from the other three, a low pass filter (LPF) is used. This signal is then ready to be sent to fourier transform and digital signal processing (DSP) circuitry for analysis and extraction of desired metrics.

2.3.3 Chirp Generation

Figure 2.5 below highlights the portion of the LADAR system being discussed in this subsection.

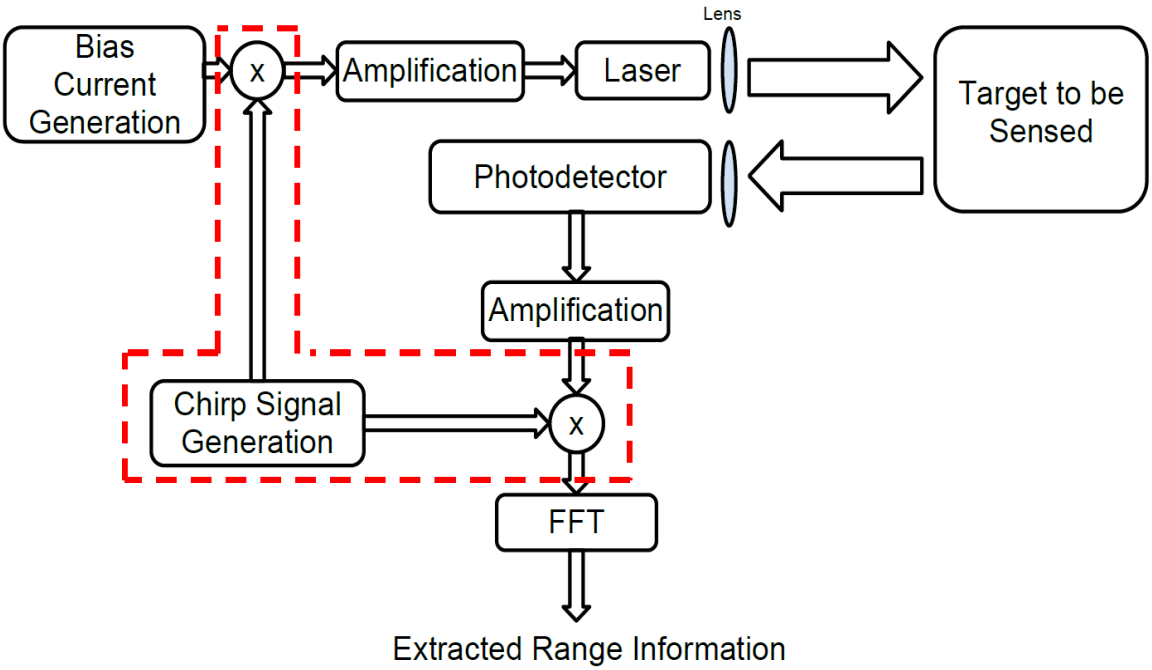


Figure 2.5: Chirp Generation Portion of LADAR System

As discussed in the two previous subsections, the chirp signal is used to modulate the bias current driving the laser. It is also used to compare to the received RF signal from the photodetector to generate the difference frequency signal of interest.

The chirp signal itself is modulated in frequency, linearly increasing from a start frequency (f_{start}) to an end frequency (f_{stop}), forming a sawtooth waveform as pictured below in Figure 2.6. The difference between the start and stop frequency is referred to as ΔF, while the difference in frequency and time between the send and receive signals are referred to as f_{if} and τ, respectively.

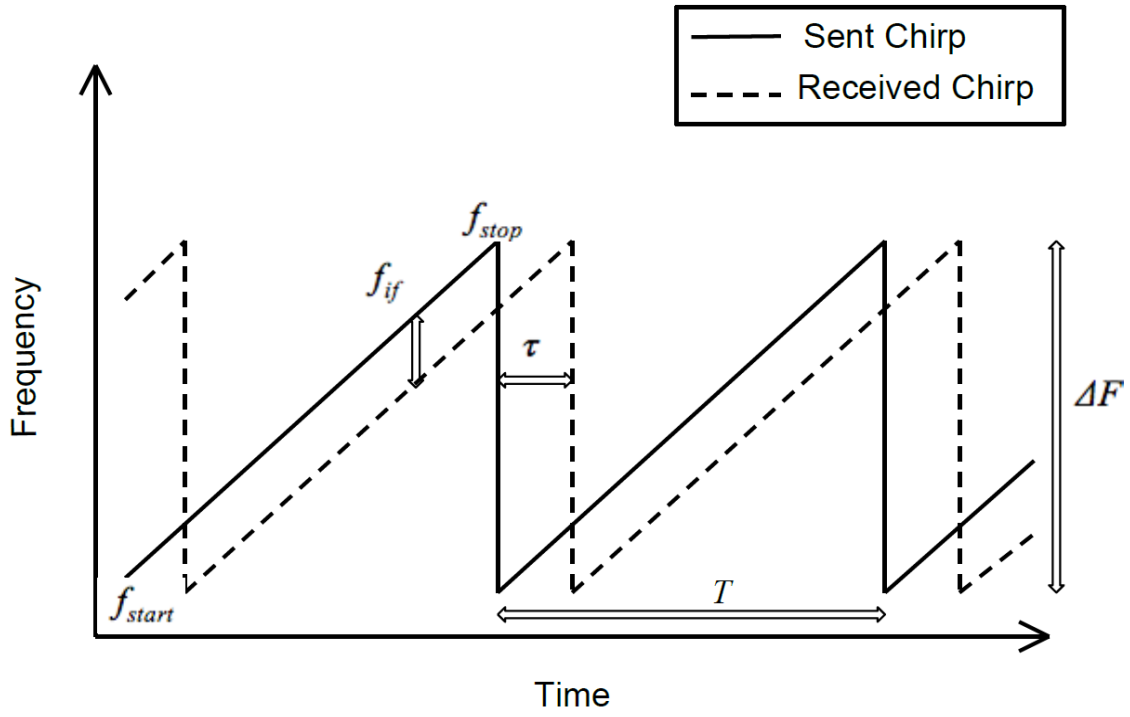


Figure 2.6: The Chirp Signal Waveform - Sent and Received

The distance to the target can be extrapolated from this data through the use of the following relationships and equations [2]:

$$f_{if} = (\Delta F/T)\tau \qquad (2.1)$$

This equation states that the difference in frequency is proportional to the time delay of the received signal compared to the sent signal, the fundamental principle that both LADAR and radar rely on in order to operate.

This time delay may be expressed as follows:

$$\tau = 2D/c \tag{2.2}$$

Where *D* is the distance to the target and *c* is the speed of the traveling light. Combining Equations (2.1) and (2.2) yields

$$f_{if} = (2\Delta F/c)(D/T), \tag{2.3}$$

which directly indicates the relationship between f_{if} and D, which is the desired metric of the LADAR system. Since the frequency range of the chirp signal, the speed of light, and the period of the chirp are all known quantities that are determined by the system designer, the distance to target can be extracted directly from the f_{if} measurement.

It is worth pointing out that there is a minimum resolution on the distance to target that can be determined from this process that can be expressed as

$$D = n\Delta R. \tag{2.4}$$

This states that the distance to target can be expressed as an integer multiple *n* times the minimum range resolution of the LADAR system, ΔR. This minimum range resolution is defined as

$$\Delta R = \frac{c}{2\Delta F}, \tag{2.5}$$

showing that the range resolution may be improved by increasing the frequency range of the chirp signal. This can be desirable based on the application, but other times a very small range resolution may not be necessary.

There is some discrepancy regarding the terminology surrounding the chirp signal. While many sources refer to this scheme of LADAR operation as being called frequency modulated continuous wave (FM CW) LADAR in the same manner as its radar counterpart, the Army Research Laboratory (ARL) frequently refers to it instead as an *amplitude* modulated (AM) chirp design.

While these two naming schemes may appear to be in contradiction of one another, they are actually both correct. The chirp signal itself is a frequency modulated signal, having it's frequency change with respect to time in a sawtooth waveform pattern as discussed previously and shown in Figure 2.6. From the perspective of biasing the laser, however, the frequency of the emitted light by the laser is constant and is a property of the laser itself. The chirp signal that is biasing the laser is actually using its amplitude to modulate the signal strength of the emitted light. So from *that* perspective, this setup can also be considered amplitude modulation.

Since it is from some perspective correct to call this LADAR scheme both amplitude modulation and frequency modulation at the same time, this document will hereby attempt to avoid confusing the reader with this seeming contradiction and refer to the AM/FM CW chirp simply as "the chirp".

2.4 LC Oscillators

Up to this point, Chapter 2 has focused on LADAR principles in general. This work, however, is primarily focused on the generation of the chirp signal. This section is intended to cover the oscillator circuits used to create this signal.

An LC oscillator is a circuit that relies on the properties of an LC tank to oscillate between a high and low voltage. LC oscillators are used heavily in RF applications because of their superior phase noise characteristics in comparison to other oscillator types such as ring oscillators [5].

2.4.1 Oscillator Basics

Oscillators are one of the most common circuit blocks used in communication systems [6]. They provide periodic signals that may be used for timing in digital circuits and for frequency translation in analog RF circuits.

When used with a mixer in RF applications, oscillators typically function to provide the LO input to the mixer (refer back to Section 2.3.2 for details in this application). This mixing allows designers to "down-convert" signals to a usable intermediate frequency or to "up-convert" signals to an RF frequency [7].

Oscillators can be used in applications that include phase locked loops (PLL), Gilbert Cells, and many other designs both analog and digital. This particular work utilizes oscillators to generate the chirp signal described in Section 2.3. For this reason, it is necessary to describe the functionality and basic design principles of oscillator circuits.

Any oscillator, regardless of its type, can be considered with respect to a positive feedback system.

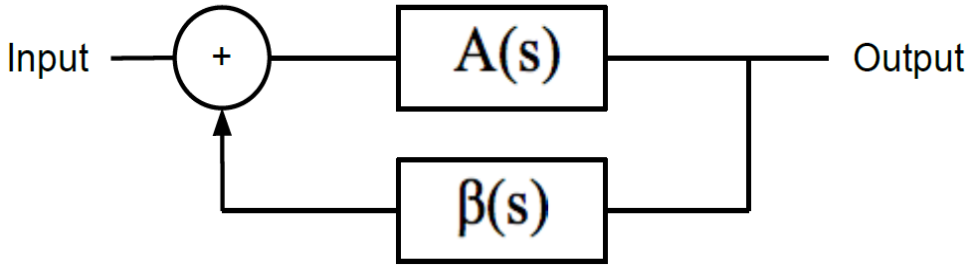


Figure 2.7: Positive Feedback Network

The transfer function of the network in Figure 2.7 can be expressed as

$$\text{Output}(s) = \frac{A(s)}{1-A(s)\beta(s)} \text{ Input}(s). \tag{2.6}$$

The Barkhousen Criterion covered in most basic circuit theory classes defines the conditions necessary for stable oscillation to occur:

$$|A(s)\beta(s)| = 1 \tag{2.7a}$$

$$\angle A(s)\beta(s) = 0° \tag{2.7b}$$

Equations 2.7a and 2.7b essentially state that the magnitude of the loop gain must be equal to unity and that the angle of the loop gain must be zero in order for stable oscillation to occur. Note that this is known as the two port feedback model because both A(s) and β(s) are shown as two port blocks making up the network.

It is also possible to express this idea in a one-port network model, shown below in Figure 2.8.

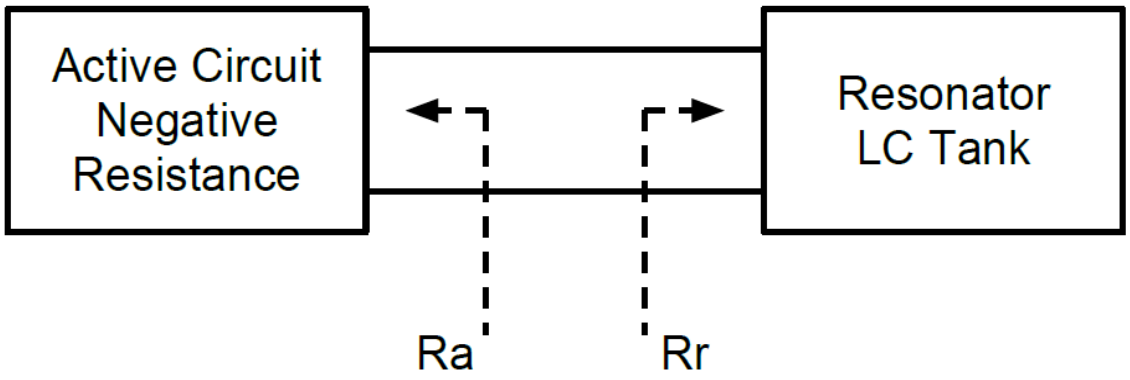


Figure 2.8: One Port Oscillator Network

This model expresses the oscillator as consisting of two separate parts— an active circuit providing a negative impedance and a resonator that consists of an LC tank. The equivalent of the Barkhousen criterion in this case is that the negative impedance seen looking into the active circuit block must be equal to the positive impedance seen looking into the resonator block [7]. In order to better understand why this is, it may be useful to consider an ideal LC resonator circuit.

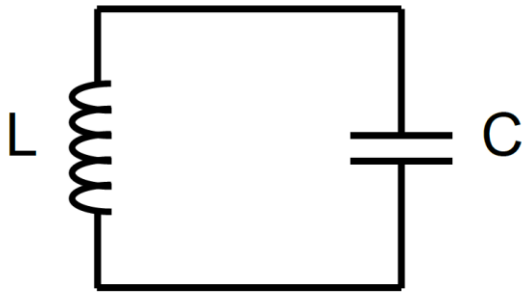


Figure 2.9: LC Resonator Circuit

If this ideal LC tank shown above in Figure 2.9 is excited with a current pulse, the energy storage properties of the inductor and capacitor will allow a fixed amount of

energy to be converted back and forth from electrical to magnetic energyfor infinite time, causing oscillation. This is only the case if the LC tank is perfectly ideal, however.

In reality, there will be a parasitic resistance associated with the components in the resonating block, and oscillation will quickly dissipate. This is why the active block is necessary to provide a negative resistance or gain in order to keep the LC tank oscillating.

If the negative resistance provided by the active circuit is sufficient to provide oscillation, then the frequency of oscillation is described by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{2.8}$$

2.4.2 LC Oscillator Topologies

The most simple implementation of the active circuit indicated in Figure 2.8 from the previous subsection is a single transistor with an LC tank. This implementation is shown in Figure 2.10a. The LC tank and direct feedback to the source terminal of the transistor are intended to satisfy the criteria for oscillation as introduced in the previous subsection.

However, the loop gain results in a value less than unity, failing to maintain oscillation [8]. The impedance transformations that occur in the feedback networks of the Colpitts and Hartley configurations, shown in Figures 2.10b and 2.11c, respectively, provide an equivalent resistance necessary to sustain oscillation.

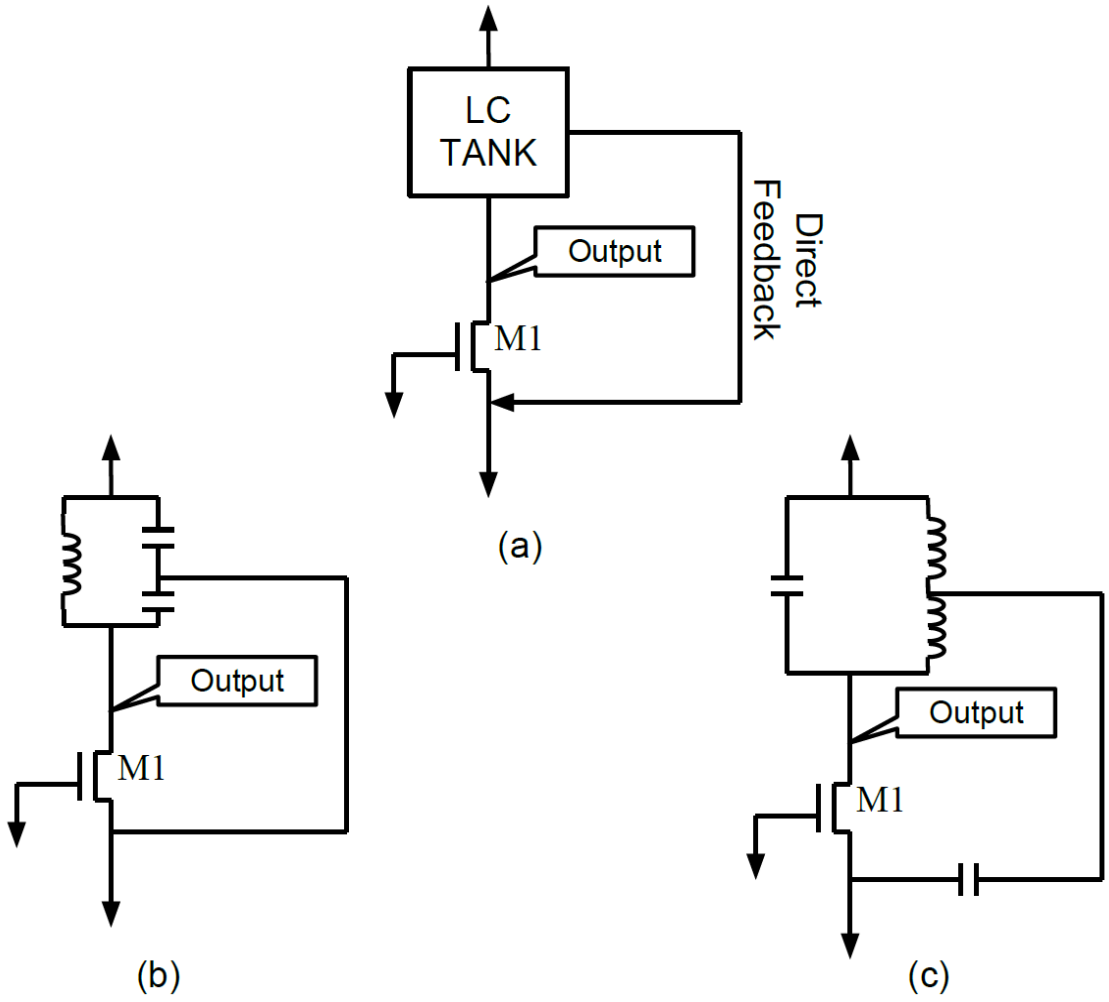


Figure 2.10: Single Transistor LC Oscillator Topologies

(a) Direct Feedback, (b) Colpitts Oscillator, (c) Hartley Oscillator

The topology shown in Figure 2.10b relies on a capacitor divider to provide the feedback while the topology in Figure 2.10c utilizes inductors to provide the feedback transformation. The Colpitts and Hartley single transistor LC Oscillators come with a host of shortcomings. The ratio of the inductors and capacitors required to attain a reasonable quality factor is relatively high, increasing chip area and cost of an IC [8]. Another drawback is that this oscillator topology has only one output.

In many applications, a cross-coupled design with a double ended output is desirable. The cross-coupled topology has the advantage of providing two symmetric outputs that are equal in magnitude but with oscillations that are 180° out of phase with each other. This topology is pictured below in Figure 2.11.

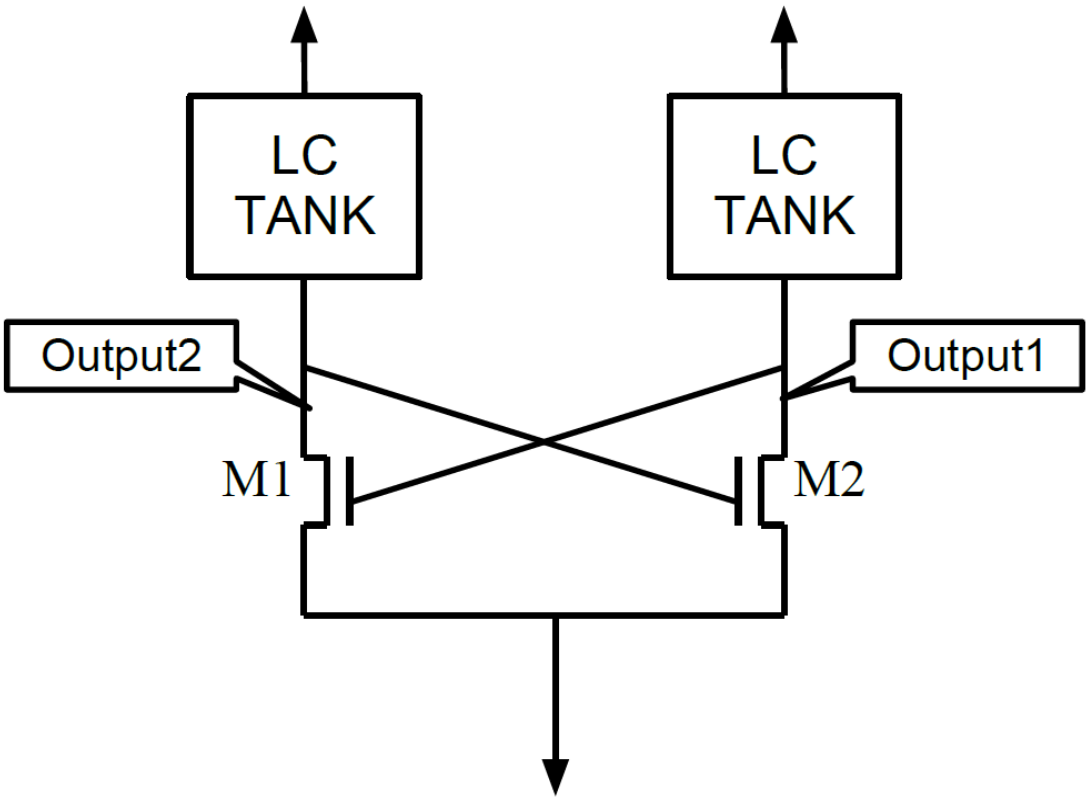


Figure 2.11: Cross-coupled LC Oscillator

When one output is high, the other is low and vice versa, as dictated by the gate voltage of each transistor being connected to the opposing output. Provided that good transistor matching between M1 and M2 is possible, then this topology offers strong symmetry. This is ideal for applications like the Gilbert cell which has a double ended local oscillator input or feeding each signal into an op-amp gain stage if desired.

The resistance seen looking into the drain terminals of M1 and M2 in Figure 2.11 must be the negative impedance discussed in Section 2.4.1. The magnitude of this impedance is equal to $2/G_M$ where G_M is defined as the transconductance, which is shown in Equation (2.9) [8].

$$G_M = \frac{\partial I_{DS}}{\partial V_{GS}}|_{Qpo\,int} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th}) \tag{2.9}$$

This topology has two notable downsides, however. There are two LC tanks in the topology as shown which requires a considerable increase in chip space and there is no improvement over the topology presented in 2.10 in terms of the negative resistance provided to ensure oscillation reliability.

Up to now, the amplitude of the oscillator has not been discussed. In the case of the two topologies presented previously, the output amplitude is a product of the drain current of the NMOS transistor and the parasitic resistance of the LC tank. That is to say, if the negative resistance provided by the transistor is enough to compensate for the parasitic resistance, oscillation will occur. If this negative resistance is large enough, the output amplitude will increase until clipping occurs due to the supply voltages. A better design includes the addition of a current source or sink included such to provide better control on the drain current flowing through each branch of the oscillator. This way, the sizing of the transistors can be tweaked to provide reliable oscillation while the current sink or source can be designed to adjust the amplitude of the oscillation. A current sink bias current is shown in Figure 2.12 as an example.

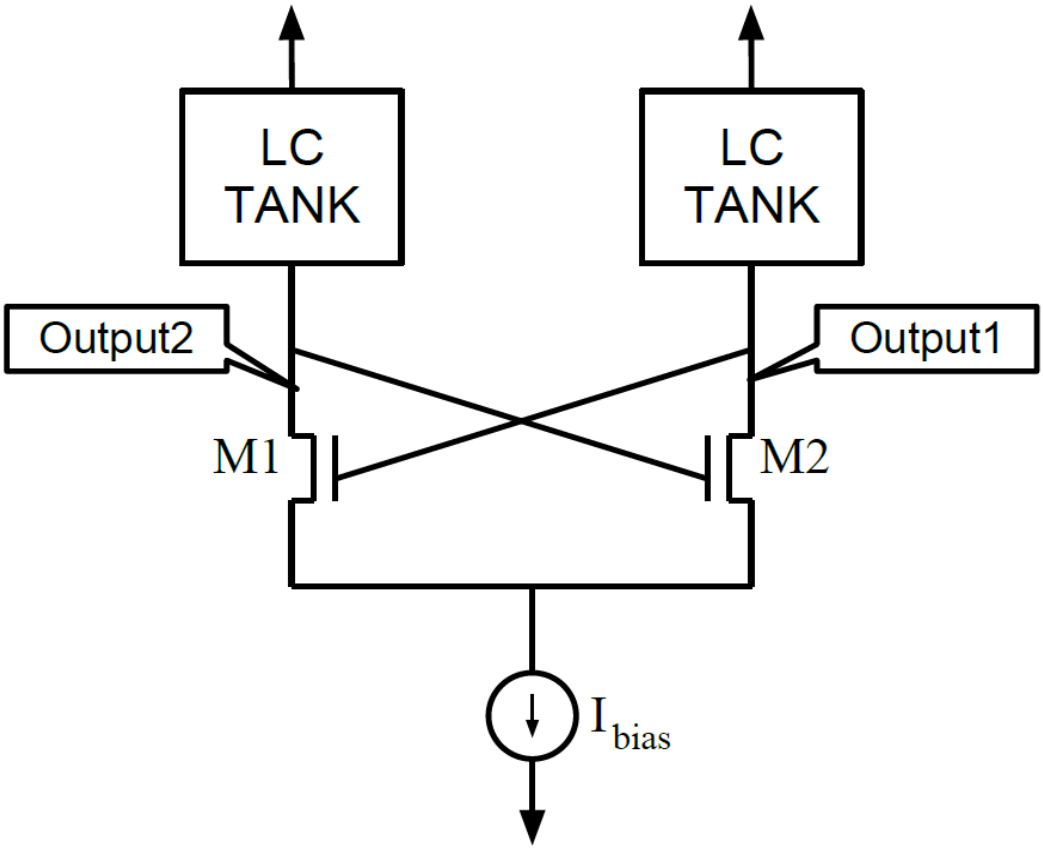


Figure 2.12: Cross-coupled LC Oscillator with Bias Current

This topology still requires two separate LC tanks, which occupies a considerable amount of die area. A better topology would be more space efficient, and also make improvements to ensure more reliable oscillation.

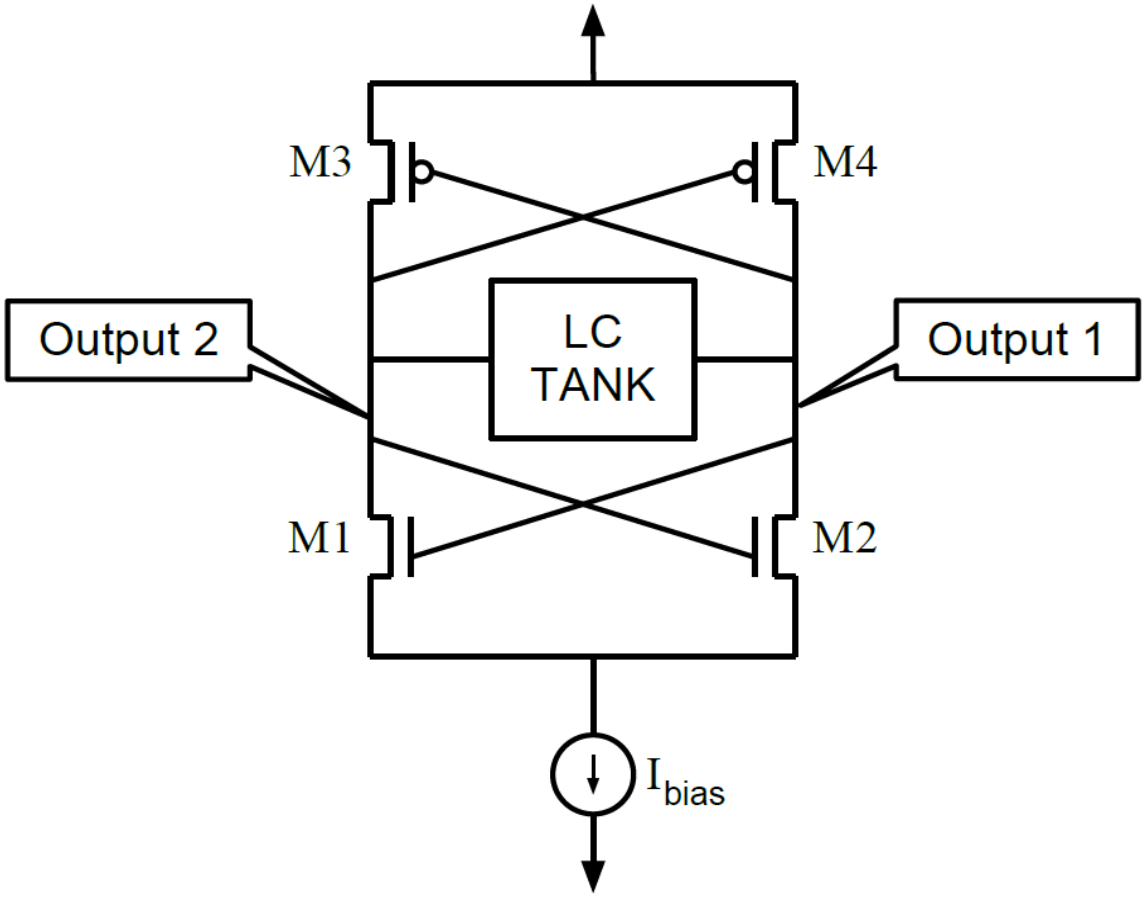


Figure 2.13: Cross-Coupled CMOS LC Oscillator

The design presented in Figure 2.13 allows for a single LC tank to be shared between each branch of the oscillator. The DC bias voltages are affected and two more transistors are now required, but the advantages are worth the small amount of additional die space in many cases. With the additional PMOS pair, the complementary topology offers higher transconductance to compensate for the resistive losses of the tank with less current consumption [6]. This allows for oscillation to occur far more easily with a variety of device sizes without the need for higher drain currents and larger transistor sizing. The topology shown in Figure 2.13 is the one utilized in this thesis work.

This concludes the technical background discussion of this thesis. The following two chapters will cover the design, layout, and test of the chips made.

Chapter 3

FIXED FREQUENCY OSCILLATOR BANK (FFOB)

3.1 Chapter 3 Introduction

The purpose of this chapter is to describe the design, simulation, layout, and testing of the first iteration of the chirp generator chip. All designs were created using the IBM CMRF7SF process. This chapter is divided into six sections. First, an overall description of the capabilities and inputs and outputs of the chip are described in Section 3.2. Next, Section 3.3 describes the design of each circuit on the schematic level. Section 3.4 describes the layout of each circuit as well as other considerations related to the layout and packaging. Section 3.5 covers the simulation results and verification of the designed circuit. Finally, Section 3.6 describes the testing of the manufactured package made by MOSIS.

3.2 Overview of the FFOB

The goal of the chip created in this work is to generate a chirp signal capable of functioning as part of a larger LADAR system as described in Chapter 2. To this end, a custom oscillator capable of outputting a signal over a wide frequency bandwidth from f_{start} to f_{stop} is desired. It is important to note that while Figure 2.6 has previously indicated that the chirp signal will consist a linearly increasing ramp up in chirp frequency, this is only an ideal model. In this design, the chirp signal produced will consist of a series of discrete frequencies created by the oscillator circuit.

These discrete frequency levels create a chirp signal that resembles a “staircase” when frequency versus time is plotted, shown conceptually in Figure 3.1, below.

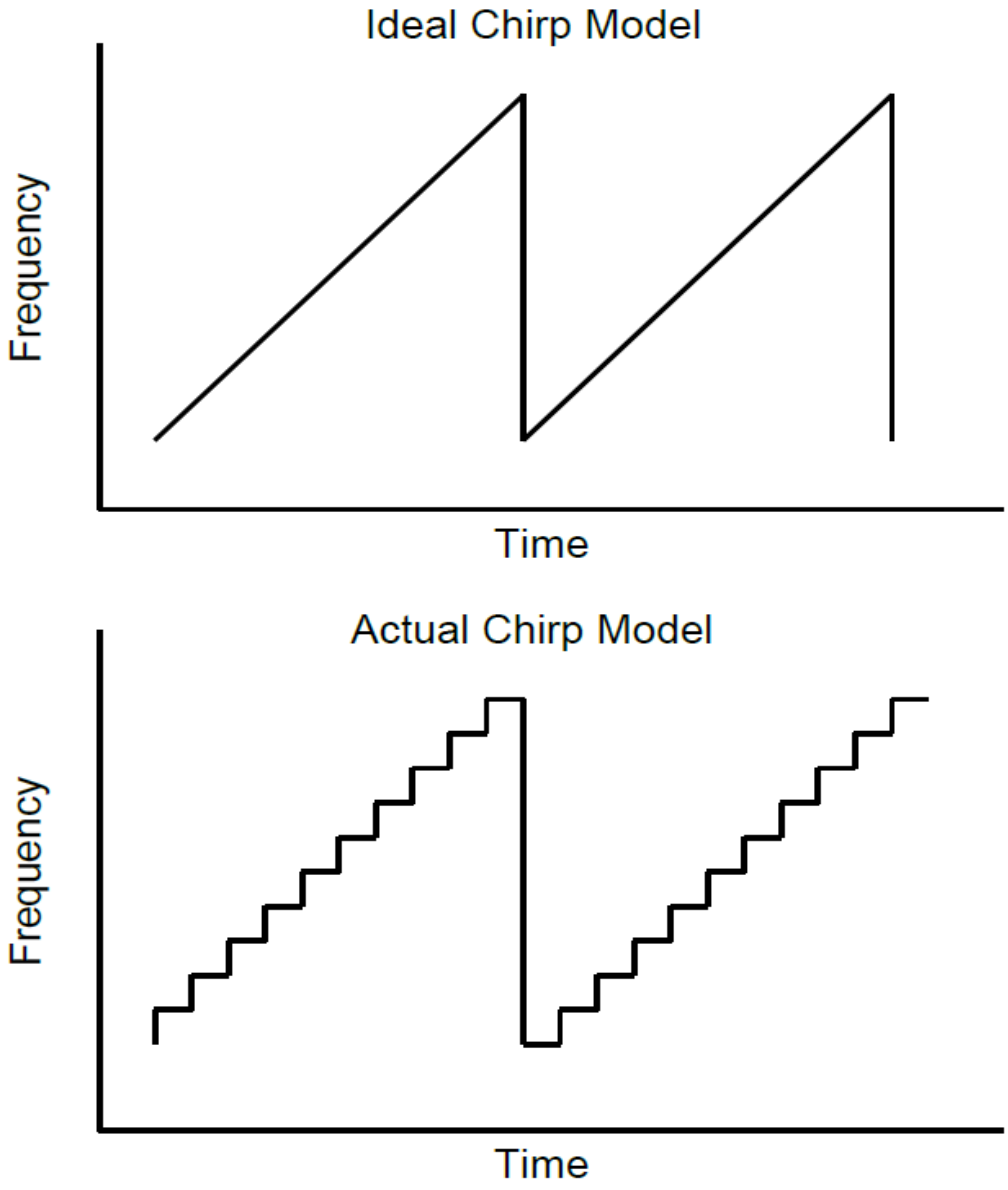


Figure 3.1: The Ideal Chirp versus the Actual “Staircase” Discrete Chirp

The parameters of interest in chirp generation of this type are the number of discrete frequencies, the span of frequencies (the bandwidth range from f_{start} to f_{stop}), and the period of the chirp. Increasing the number of discrete frequencies increases the accuracy of the LADAR system and also increases the energy of the usable output signal of the system by providing more intermediate frequency peaks per chirp period. Increasing the bandwidth improves the range resolution of the system. The chirp period must be such that the chirp signal works with respect to the overall system design with how fast the signal processing and other system functions take place.

The FFOB includes a simple, straightforward design with no clock signals controlling the oscillator functionality. Sixteen discrete frequencies are output from the chip, and their frequency values are fixed. Each oscillation frequency is controlled by it's own input pin. Oscillation frequencies range from 600 MHz to 2.1 GHz at intervals of 100 MHz. This represents a total bandwidth of 1.5 GHz. Recall from Chapter 2 that the overall range resolution is given by

$$\Delta R = \frac{c}{2\Delta F}. \tag{3.1}$$

For this design, solving for the range resolution in this case yields:

$$\Delta R = \frac{3\times10^{8}\,\mathrm{m/s}}{2\cdot 1.5\,\mathrm{GHz}} = 0.10\mathrm{m} \tag{3.1}$$

This means that the range resolution of a LADAR system operating with this chirp signal is 10 cm which represents the minimum range difference that the system is able to distinguish. The chirp period is not produced on chip. Off chip circuitry is required to determine the chirp period as each oscillator is controlled by an external signal through an input pin.

Figure 3.2 is presented below to give an overview of the inputs and outputs of the FFOB design. There are sixteen total input control pins each controlling which oscillation frequency is sent to the single output pin, in addition to power and ground pins. It is left to the user to ensure that no more than one oscillator is turned on simultaneously, which represents a clear drawback of this design. The shortcomings of this design are explained in Chapter 4, along with how they are addressed in the VCOB design.

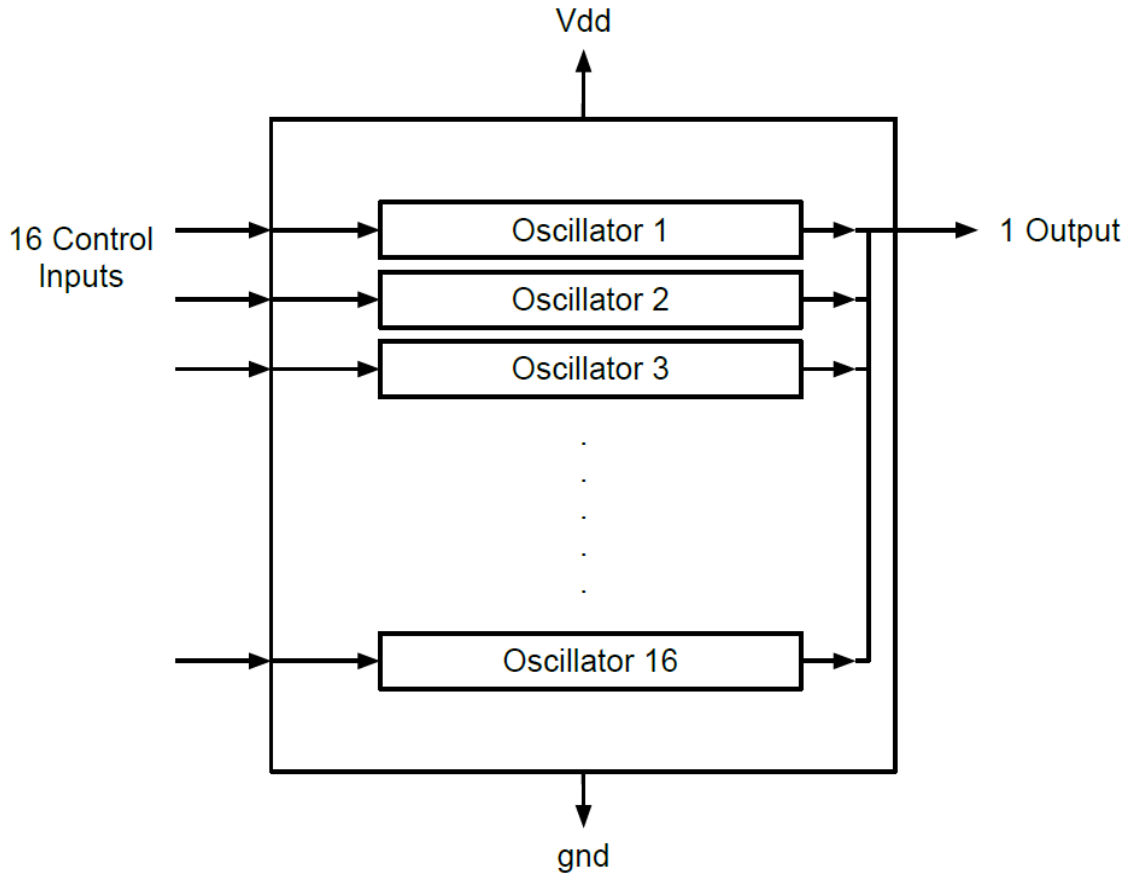


Figure 3.2: Overview of Inputs and Outputs in the FFOB Design

3.3 Design and Schematics

The design of each individual circuit block of the FFOB are each described in the following subsections, with schematics and descriptions of how each circuit block interfaces with the rest of the chip being provided.

3.3.1 The Fixed Frequency Oscillator

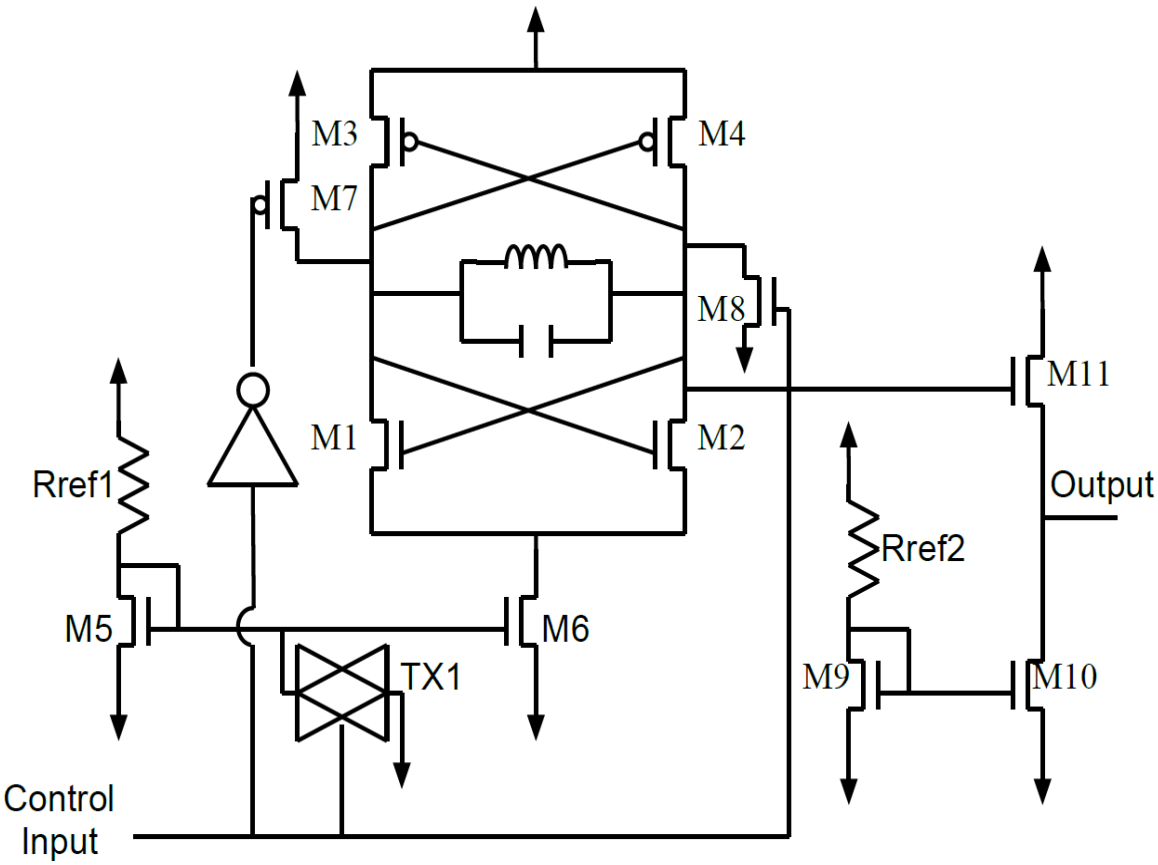


Figure 3.3: The Oscillator Schematic

Figure 3.3 shows an example of one of the sixteen oscillators used in the FFOB design. The circuit is similar to the one described in Section 2.4.2, with a few notable additions. A 3.3V supply is used in this design. There is a pull-up PMOS transistor tied to the unused output and a pull-down NMOS transistor tied to the primary output. These transistors are meant to be in the "ON" state whenever this oscillator is inactive, thus

providing the necessary startup circuitry to ensure that the initial conditions of the oscillator are such that the two outputs begin at opposite voltages. There is a control input on each oscillator that determines whether or not it is active that is meant to be controlled with an off-chip high or low voltage.

When the control bit is off, a transmission gate is used to ground the gate connection on the NMOS current mirror that supplies current to the oscillator. This transmission gate will be described in Section 3.3.2. The transmission gate is used to cut off all current to the unused oscillator and thus stopping oscillation on the output and reducing power consumption.

Also shown in Figure 3.3 is the output stage connected to one of the two symmetric outputs of the oscillator. This output stage consists of a single source follower current gain stage that is intended to allow the oscillator to drive a 50 Ohm load with a sufficient power. The output stage is driven by an NMOS current sink similar to the one that drives the oscillator. Note that each and every oscillator in this design has its own output stage. The advantage of this is the ability to size the source follower NMOS transistor differently for each oscillator to achieve uniformity in terms of output current magnitude from oscillator to oscillator.

Table 3.1: Oscillator Component Values

Oscillator Name	Desired Frequency	L (nH)	C (pF)
oscillator600meg	600 MHz	15.0	3.65
oscillator700meg	700 MHz	15.0	2.45
oscillator800meg	800 MHz	10.1	3.10
oscillator900meg	900 MHz	10.1	2.28
oscillator1000meg	1.0 GHz	10.1	1.80
oscillator1100meg	1.1 GHz	10.1	1.41
oscillator1200meg	1.2 GHz	10.1	1.16
oscillator1300meg	1.3 GHz	10.1	0.890
oscillator1400meg	1.4 GHz	10.1	0.720
oscillator1500meg	1.5 GHz	10.1	0.550
oscillator1600meg	1.6 GHz	10.1	0.432
oscillator1700meg	1.7 GHz	10.1	0.332
oscillator1800meg	1.8 GHz	10.1	0.240
oscillator1900meg	1.9 GHz	10.1	0.158
oscillator2000meg	2.0 GHz	10.1	0.075
oscillator2100meg	2.1 GHz	10.1	0.050

The LC tank in the FFOB is made up of one inductor and once capacitor. Values for these components are shown in Table 3.1. Alternative options were explored to avoid using sixteen oscillators to generate sixteen different frequencies. Switching in additional capacitors to modify the size of the LC tank was considered, but was ultimately discarded. The parasitic capacitances associated with switching in parallel capacitors proved to be too significant in relation to the magnitude of the capacitances being switched in, which were on the order of femto Farads.

The inductors used were typically quite large compared to the capacitors, as seen in Table 3.1. This is because the inductors have a narrow region in sizing where the peak Q value corresponds with the frequency of operation. It is much more effective to adjust the capacitance values and leave the inductance fixed to achieve small tuning changes in frequency.

3.3.2 Transmission Gate

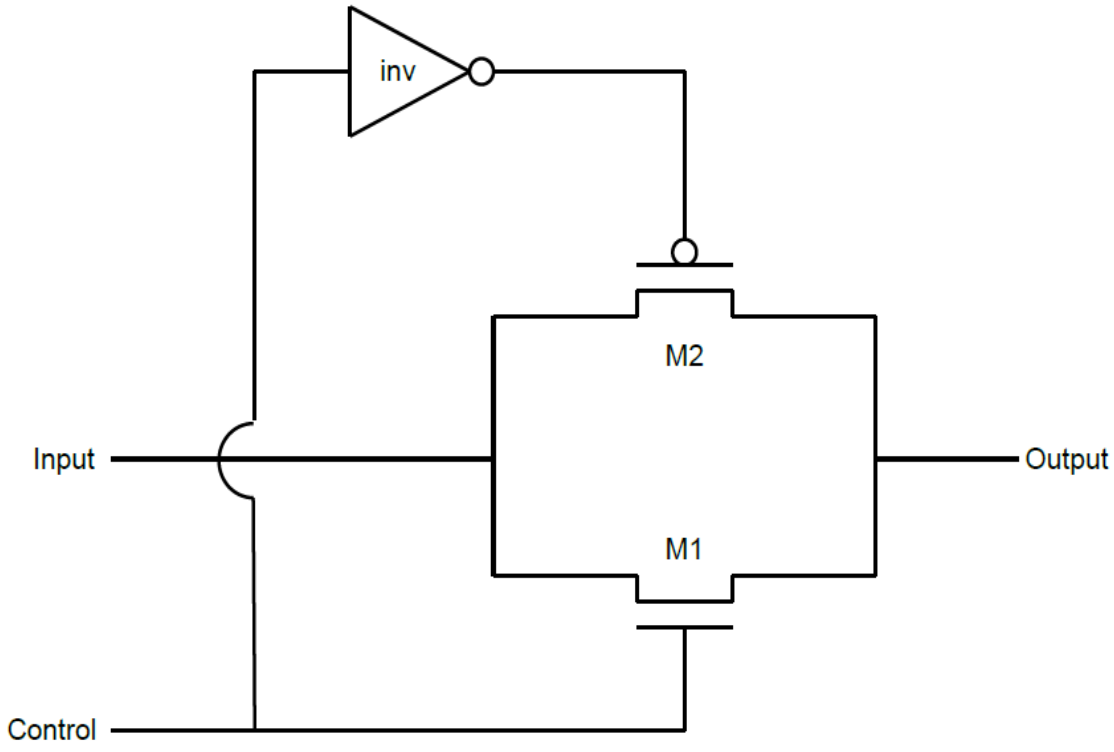


Figure 3.4: Transmission Gate Schematic

The schematic of the transmission gate introduced in the previous section is shown above in Figure 3.4. The purpose of this circuit is to short the gates of the current sink driving the oscillator to ground whenever the the transmission gate is in the "ON" state, thus removing the current source from the oscillator. The NMOS and PMOS transistors in this circuit are sized equally and are designed to accommodate currents in the 30 to 40 mA range, which is the peak current through any branch of the oscillator circuit.

Each oscillator with its output stage is tied together into a single final output, as shown below in Figure 3.5. The transmission gates in each oscillator block were designed to prevent current being output by any oscillator in the "OFF" state, such that only one oscillator would ever have an output current at any particular time, as controlled by the input pins ctrl 1 to ctrl 16.

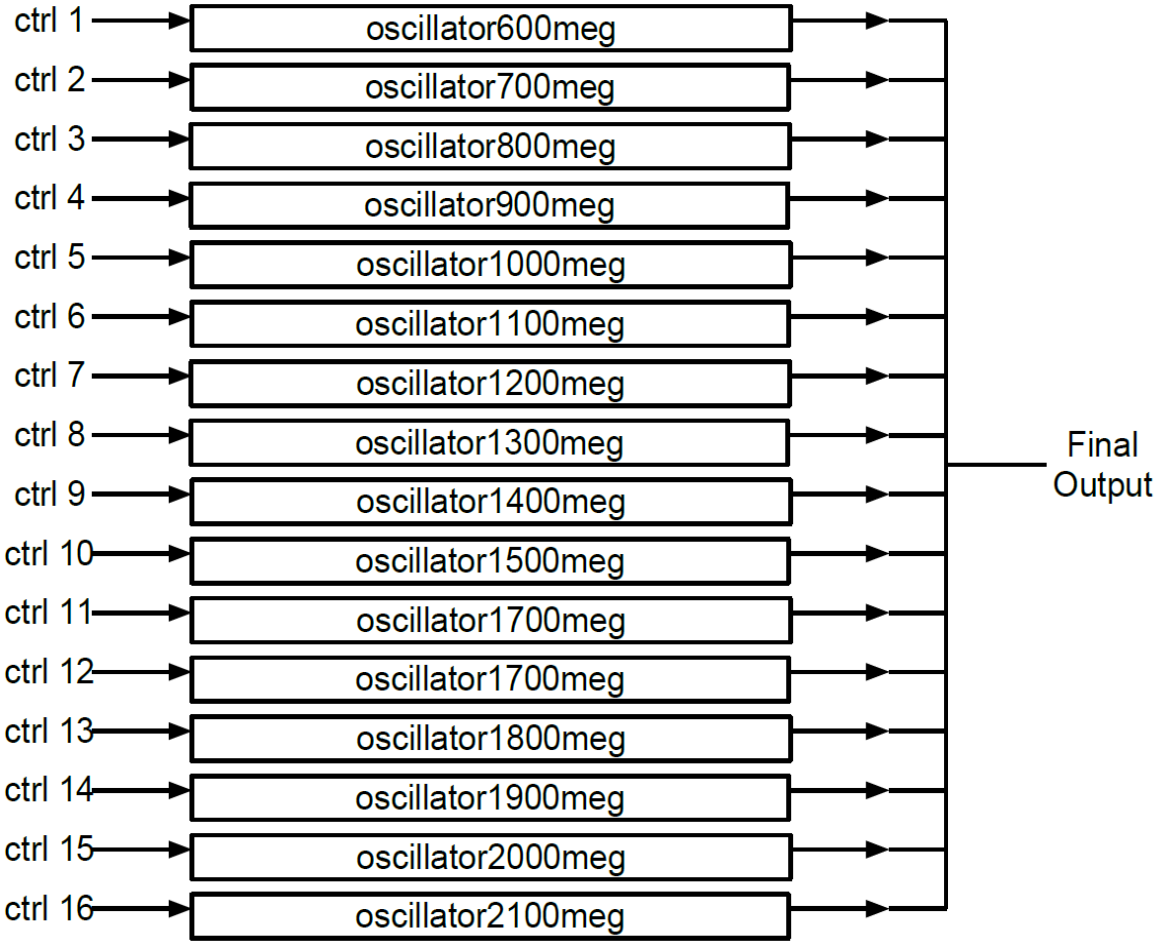


Figure 3.5: All Sixteen Oscillators with Outputs Tied Together

3.4 Layout and Packaging

Each input and output pin on the package needs electrostatic discharge (ESD) protection interfacing between the circuit and the package pads. Figure 3.6 shows the ESD devices, consisting of two sets of two reverse biased diodes with a single resistor between the two devices. These devices are used to prevent a static discharge caused by a human inadvertently touching the leads of the device without being properly grounded.

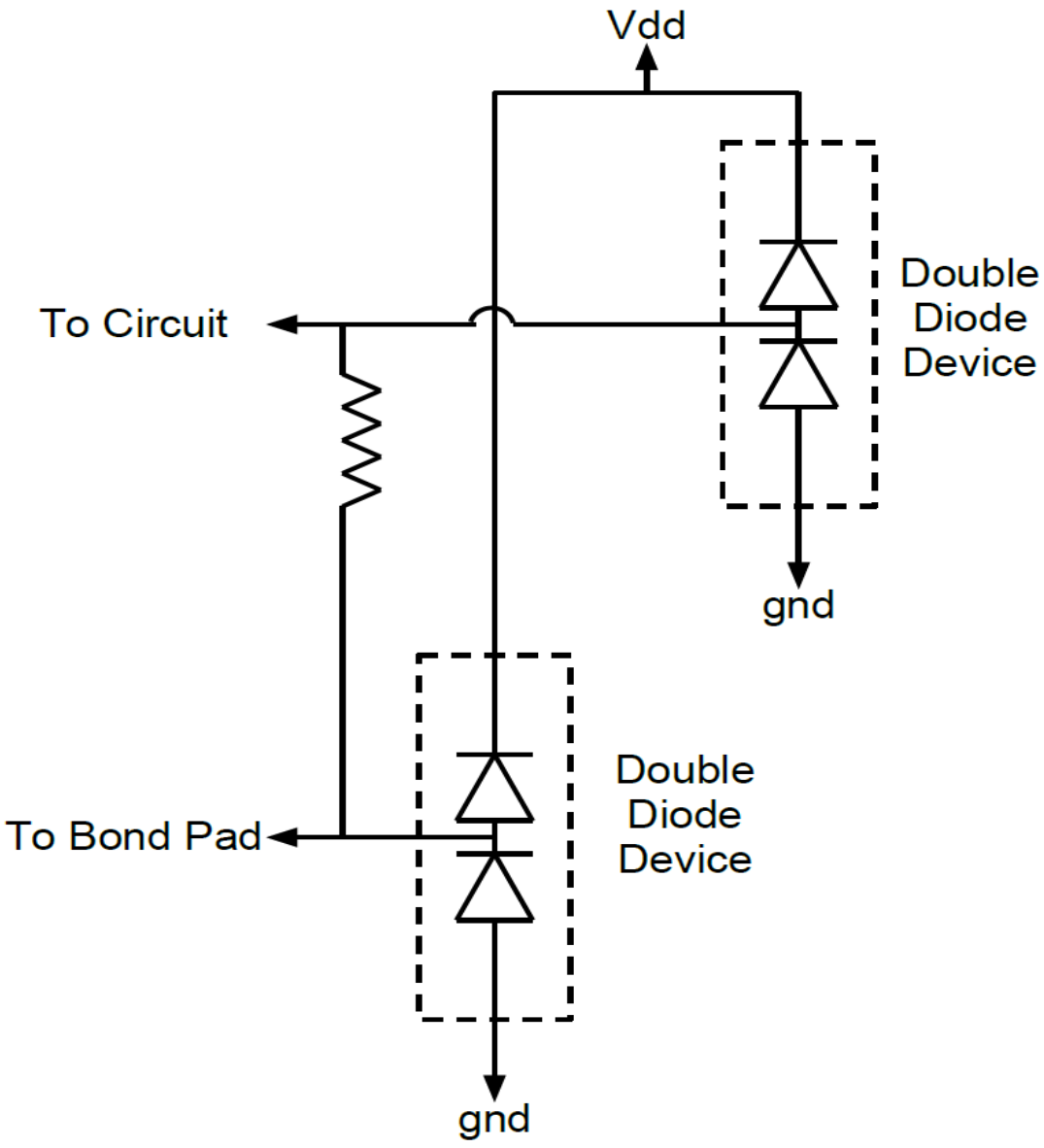


Figure 3.6: ESD Schematic

Figure 3.7 shows the layout view of one of the oscillators. The majority of the space is used by the inductor, occupying 165µm by 170µm. The next largest components are the output source follower (100µm by 10µm) and the capacitor (34µm square). The wires are also quite wide (as large as 20µm wide) and occupy multiple layers of metal in parallel in most cases in order to accommodate large currents that range up to 30 to 40 mA. There is a grounded metal layer in between the two oscillator output signal wires to prevent crosstalk.

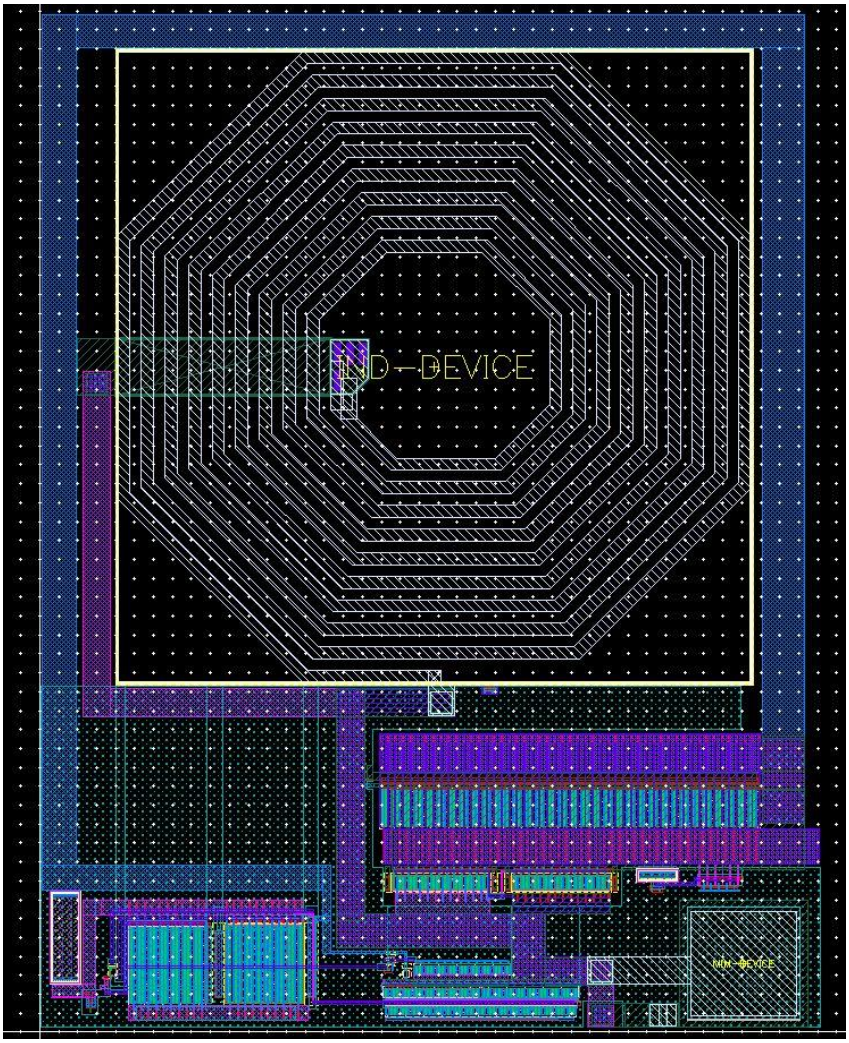


Figure 3.7: The Oscillator Layout

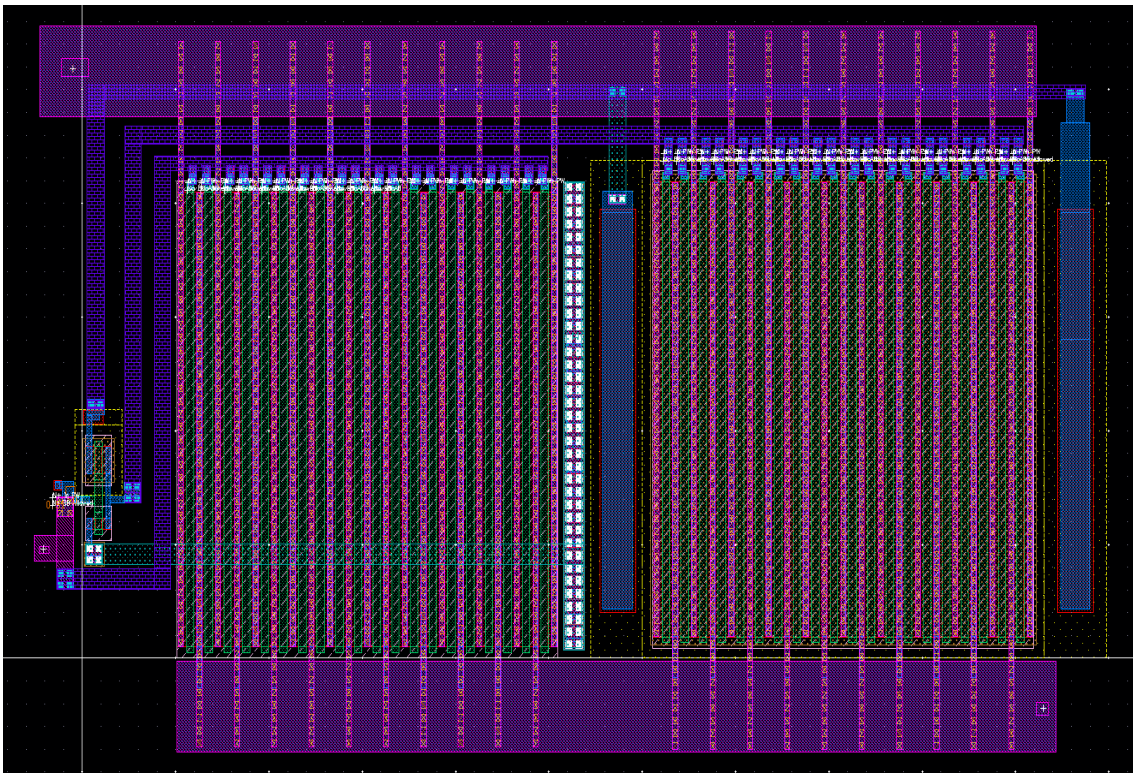


Figure 3.8: Transmission Gate Layout

A view of the transmission gate layout is seen in Figure 3.8, above. The transmission gate occupies a 55µm by 30µm space, compared to the 200µm by 270µm area that is occupied by one full oscillator in the FFOB.

Figure 3.9, provided below, shows the layout of the ESD devices included on all input and output pins in the final package. This block occupies 200µm by 115µm, but is placed underneath bond pads to conserve space.

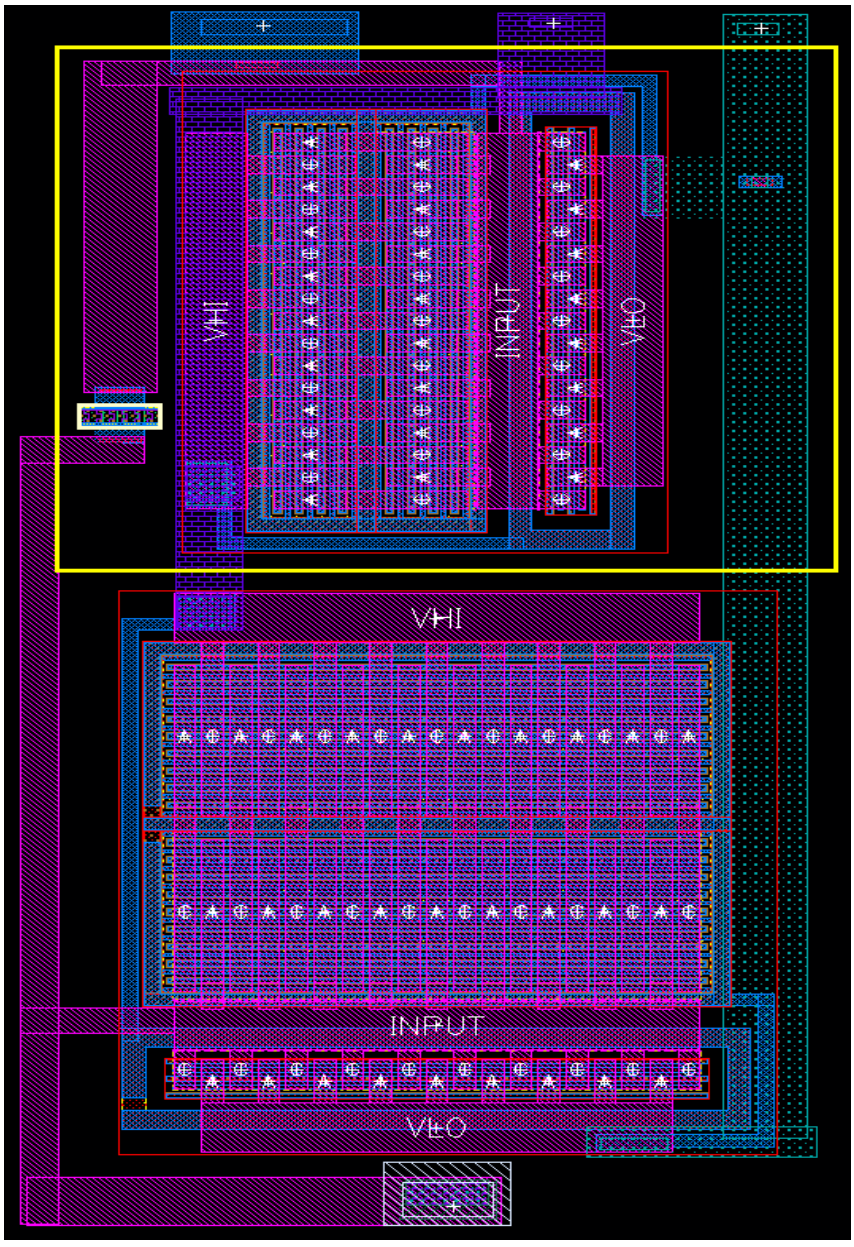


Figure 3.9: ESD Layout

The complete FFOB layout is shown in Figure 3.10. The complete package dimensions are 1500µm by 1500µm.

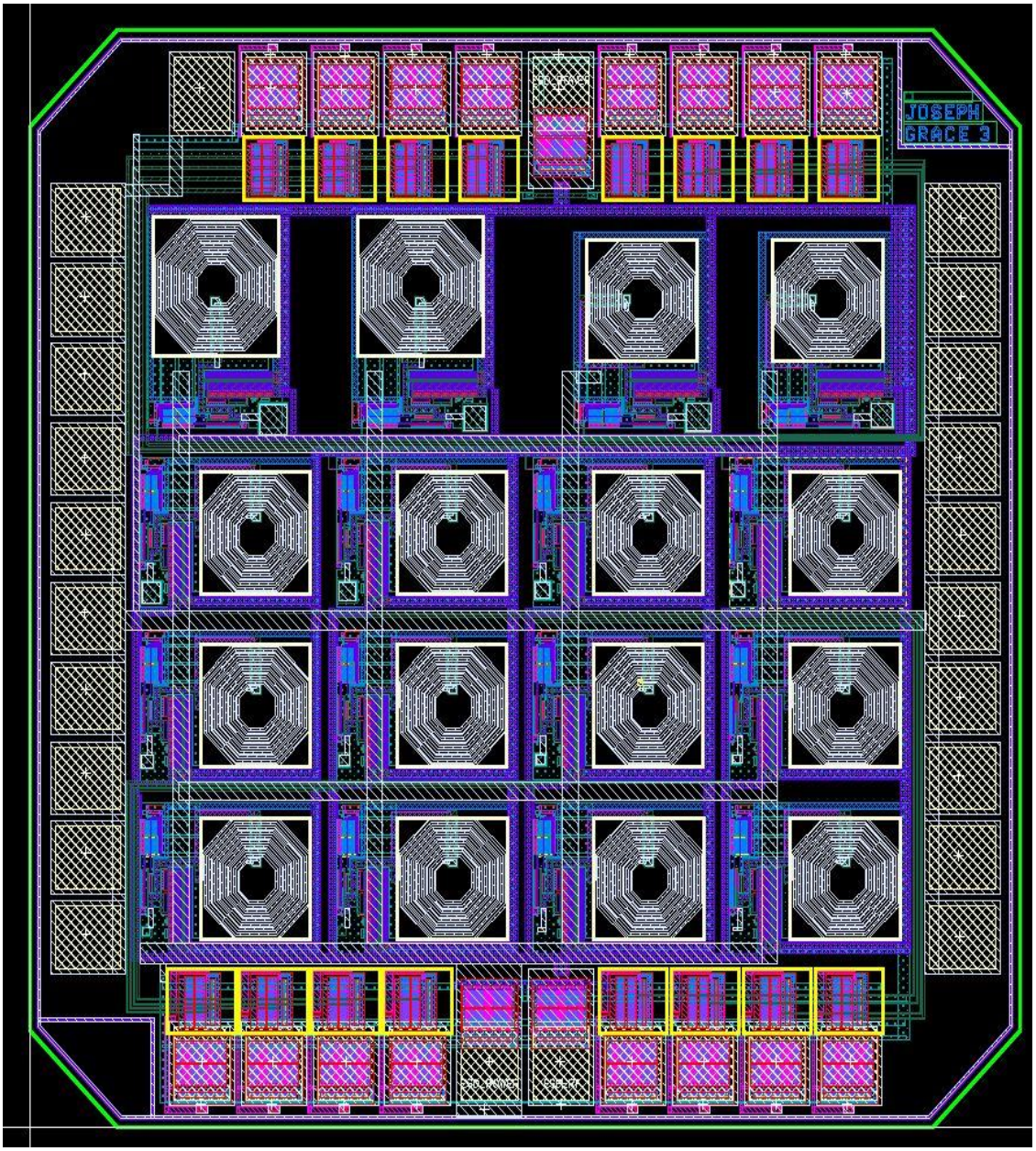


Figure 3.10: Complete Layout of the FFOB

The complete layout includes 16 oscillators. Half of the space occupied by each ESD circuit is located underneath the bond pads to conserve space. The output of each oscillator ranges into the tens of milliamps, requiring significant space to be occupied by wide metal wire connections.

Information detailing the package characteristics is provided in Figure 3.11, taken directly from the package handbook provided by MOSIS for the DIP-40 package used for this design. Each package pin has parasitic lumped element values that have been modeled as shown.

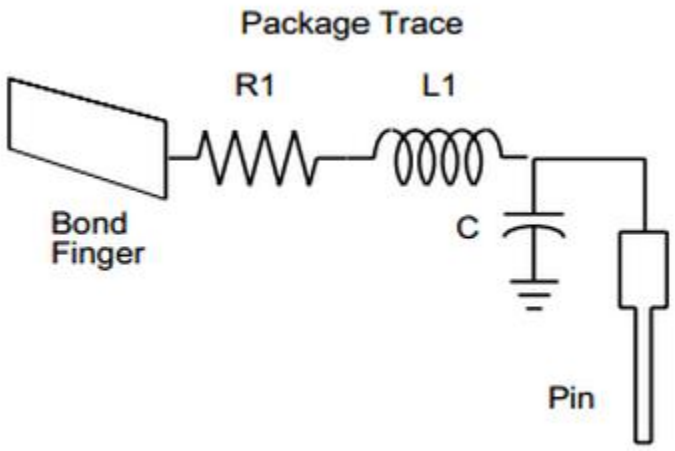


Figure 3.11: Packaging Parasitics Model

Table 3.2: Package Pinout

PINOUT				
pin name	**pin number**	**R (Ohms)**	**L (nH)**	**C (pF)**
output	31	0.0247	3.15	0.66
ctrl1	6	0.0661	4.37	1.43
ctrl2	7	0.0646	4.54	1.48
ctrl3	8	0.0498	3.69	1.05
ctrl4	9	0.0378	3.54	0.863
ctrl5	11	0.0247	3.15	0.66
ctrl6	12	0.0378	3.54	0.863
ctrl7	13	0.0498	3.69	1.05
ctrl8	14	0.0646	4.54	1.48
ctrl9	35	0.0661	4.37	1.43
ctrl10	34	0.0646	4.54	1.48
ctrl11	33	0.0498	3.69	1.05
ctrl12	32	0.0378	3.54	0.863
ctrl13	29	0.0378	3.54	0.863
ctrl14	28	0.0498	3.69	1.05
ctrl15	27	0.0646	4.54	1.48
ctrl16	26	0.0661	4.37	1.43
vdd	10	0.0247	3.15	0.66
ground	30	0.0247	3.15	0.66

Table 3.2 provides a complete list of all of the pins used in this iteration of the design, as well as the parasitic component values associated with each pin. There are sixteen control inputs, one output, power, and ground for a total of nineteen used pins on the 40 pin dual in-line package (DIP). Pins were chosen to minimize the effects of package parasitics, which are provided in terms of their component values per pin in the table. These parasitics as well as post-layout extraction parasitics are all included in the simulation data in the following section.

3.5 Simulation and Verification

The circuit was verified through simulation in the Cadence design environment. All simulations provided in this section include both the package parasitics and the post-layout extraction parasitics. Final output frequencies are provided in the table, below.

Table 3.3: Simulated Output Frequencies

Oscillator Name	Desired Frequency	L (nH)	C (pF)	Observed Frequency
oscillator600meg	600 MHz	15.0	3.65	606 MHz
oscillator700meg	700 MHz	15.0	2.45	704 MHz
oscillator800meg	800 MHz	10.1	3.10	806 MHz
oscillator900meg	900 MHz	10.1	2.28	909 MHz
oscillator1000meg	1.0 GHz	10.1	1.80	1.01 GHz
oscillator1100meg	1.1 GHz	10.1	1.41	1.11 GHz
oscillator1200meg	1.2 GHz	10.1	1.16	1.20 GHz
oscillator1300meg	1.3 GHz	10.1	0.890	1.31 GHz
oscillator1400meg	1.4 GHz	10.1	0.720	1.41 GHz
oscillator1500meg	1.5 GHz	10.1	0.550	1.51 GHz
oscillator1600meg	1.6 GHz	10.1	0.432	1.63 GHz
oscillator1700meg	1.7 GHz	10.1	0.332	1.73 GHz
oscillator1800meg	1.8 GHz	10.1	0.240	1.81 GHz
oscillator1900meg	1.9 GHz	10.1	0.158	1.94 GHz
oscillator2000meg	2.0 GHz	10.1	0.075	2.08 GHz
oscillator2100meg	2.1 GHz	10.1	0.050	2.12 GHz

The observed frequency column represents the final simulated values output from the chip driving a 50 Ohm load. The L and C columns are the values of the inductor and capacitor used in each LC tank in the FFOB.

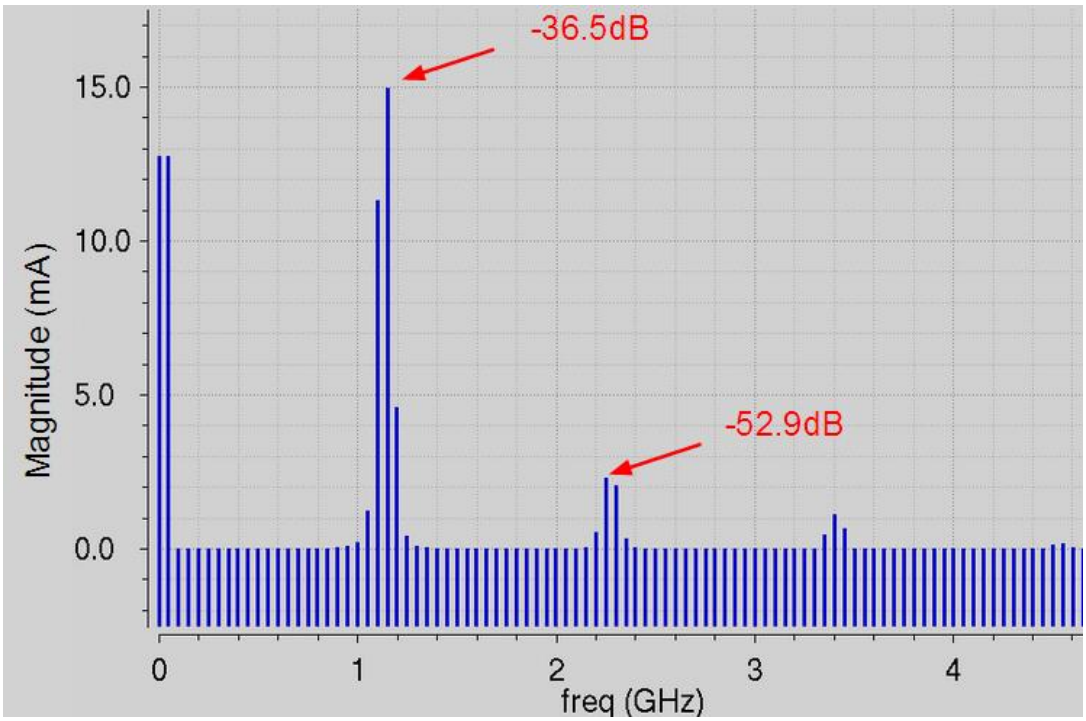


Figure 3.12: 1100 MHz Output

The 1100 MHz oscillator output is shown as simulated, with a fourier transform applied within the Cadence design environment. The dominant peak is at the desired frequency near 1100 MHz, but there are also additional frequency components at each multiple of the desired frequency. There is also a significant component at very low frequency. This results in a distortion of the sine wave, which can be visualized in a standard transient simulation plot provided in Figures 3.13 and 3.14.

Figure 3.13, provided below, illustrates the time domain output of the 1100 MHz oscillator transitioning to the 1200 MHz oscillator after running for 50 ns. Notice that the oscillation starts up and stabilizes in less than less than 10 nanoseconds. This value will dictate the overall chirp period specification chosen by the end user of this chip. Each oscillator needs to be on for at least 30-50 ns to ensure that the transition periods switching from one frequency to the next are not significant with respect to the overall chirp period. Since chirp periods are usually on the order of hundreds of microseconds to the millisecond range, this lower limit on the chirp period specification is acceptable.

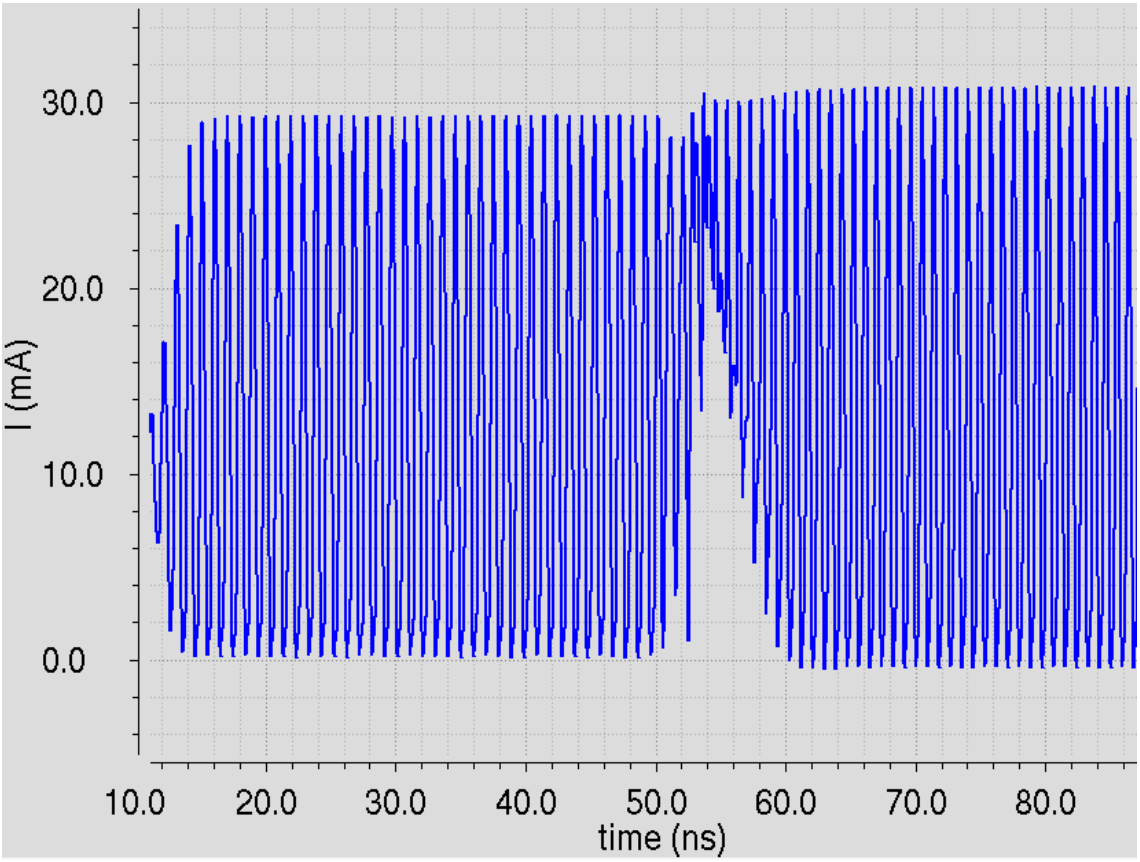


Figure 3.13: Oscillator Transition Simulation

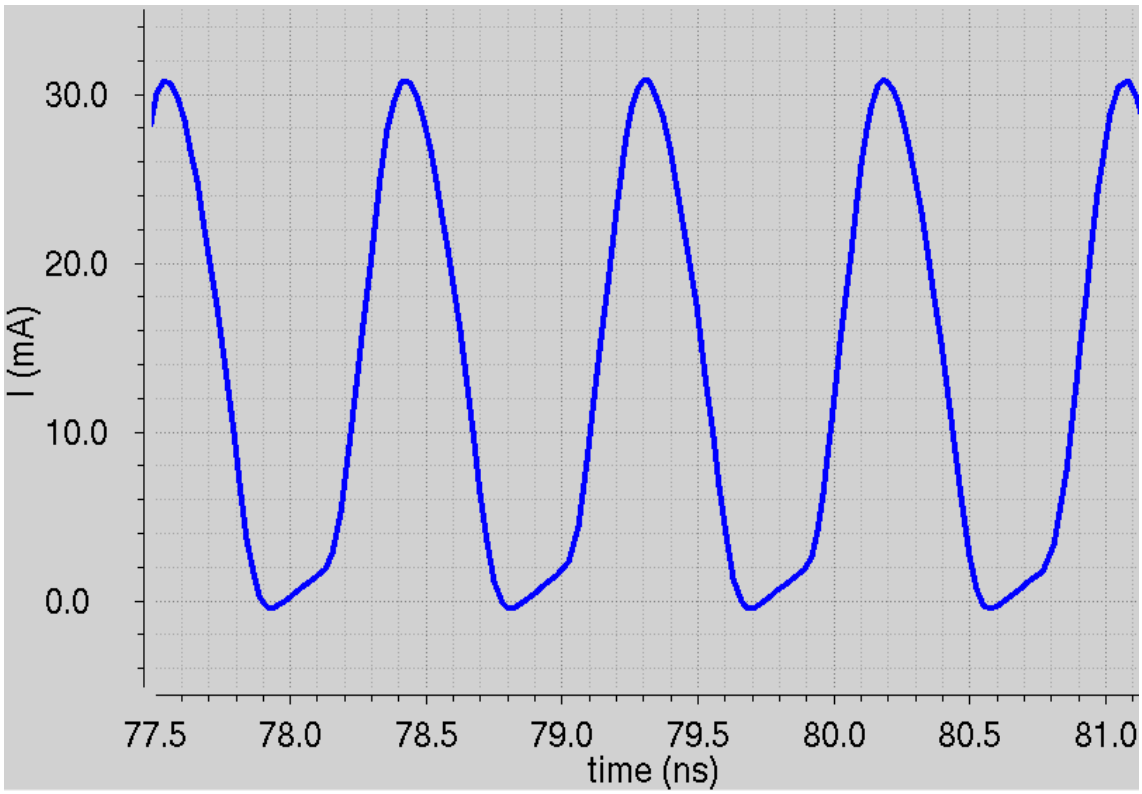


Figure 3.14: 1100 MHz Oscillator Transient Simulation Zoomed

The above figure shows a transient simulation of the 1100 MHz oscillator driving a 50 Ohm load, zoomed in to see the shape of the periodic waveform generated. The distortion discussed in relation to Figure 3.12 is evident in this image, as well. While a perfect sinusoid is prefered, the signal shown has sharper upper peaks than lower minima, which is a product of the additional frequency components contributing to distortion. The two primary causes are saturation from operating the LC oscillator too close to the supply rails and poor matching of the oscillator output to the linear operating range of the source follower output stage. This problem is addressed in the new revision of the chip, the VCOB, described in Chapter 4.

3.6 Testing the Manufactured Chip

The FFOB was sent to MOSIS for manufacturing, and a PCB was designed in ExpressPCB to test its functionality. A 3.3V voltage regulator was included to provide a consistent supply voltage for the chip, while two switches were utilized to control the delivery of power to each circuit component. A PIC18 microcontroller was used to toggle each control pin on the oscillator. The PIC was chosen due to its simplicity and the designer's past experience in it's programming.

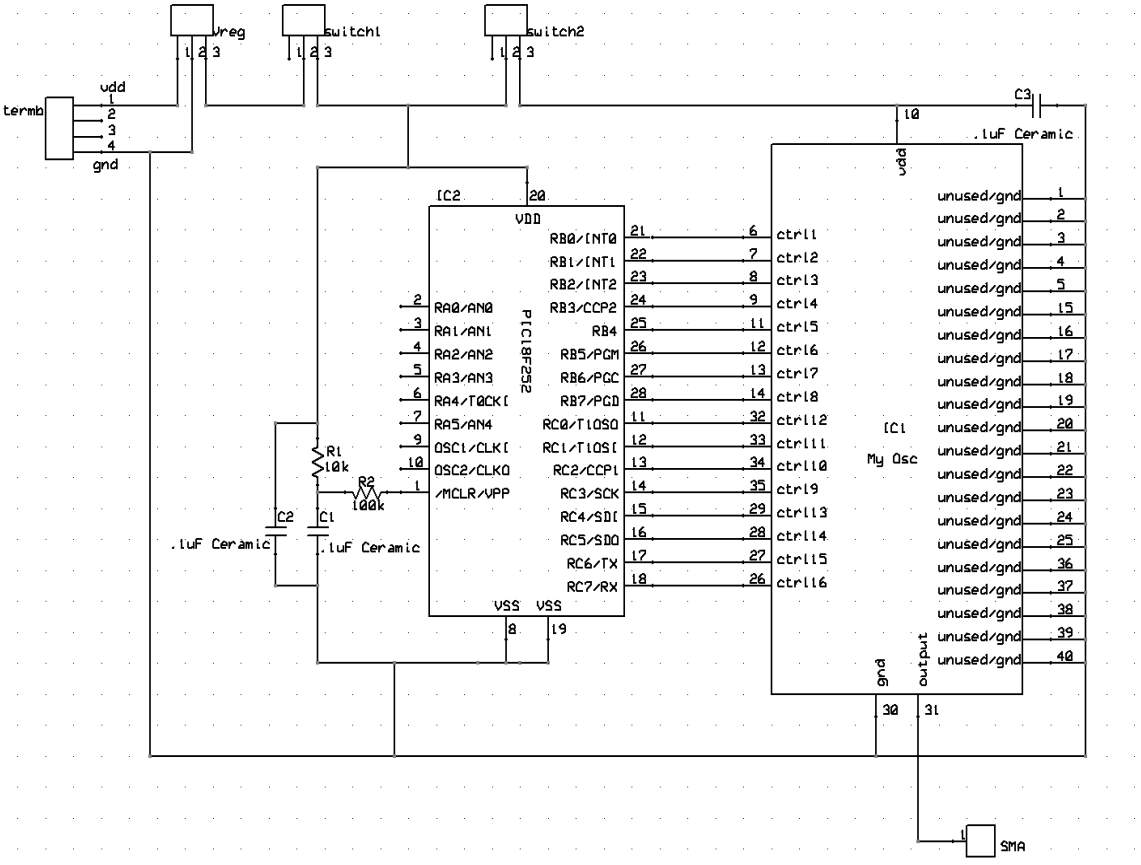


Figure 3.15: Test PCB Schematic

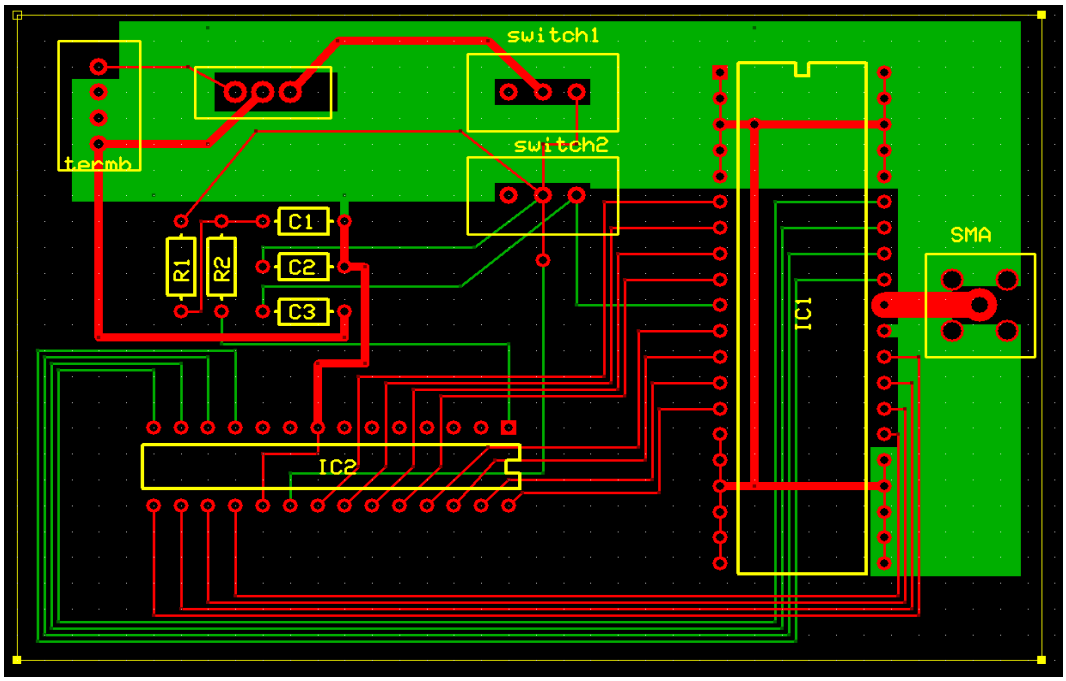
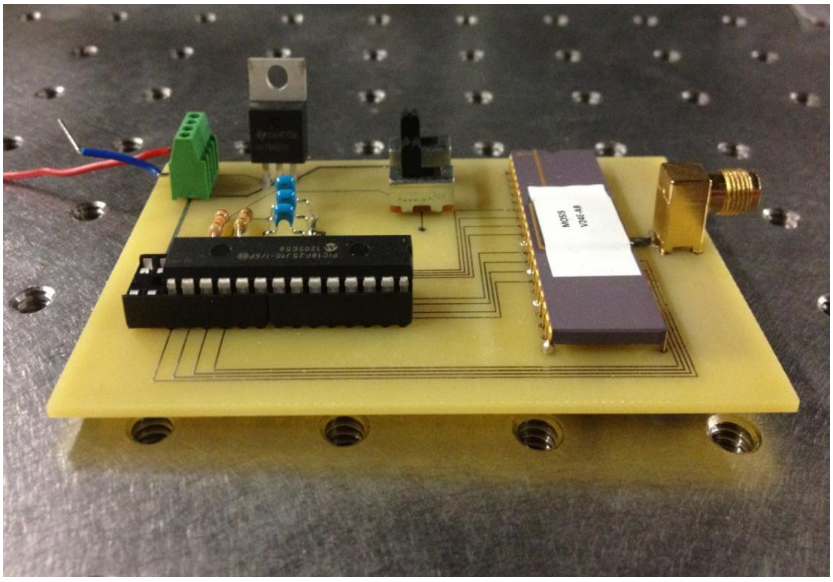


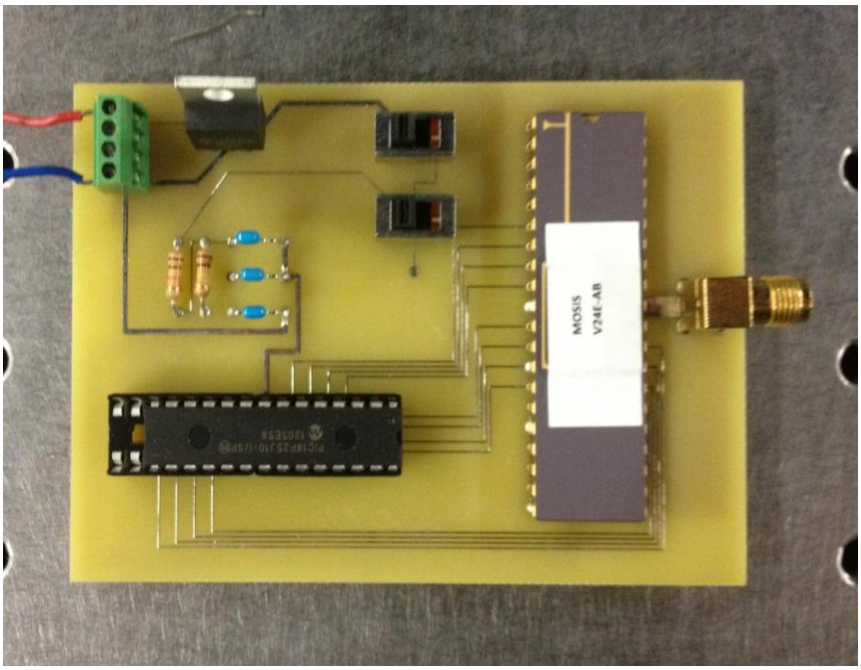
Figure 3.16: Test PCB Layout

Figure 3.16, presented above, displays the layout of the test board as designed in ExpressPCB. A 2-layer board was chosen for simplicity, with commercial off the shelf metal film resistors and ceramic resistors used. The output pin was tied to an SMA connector to accommodate high frequency signals.

Figures 3.17a and 3.17b provide photographs of the manufactured test setup with the IC soldered onto the board.



(a)



(b)

Figure 3.17: Photographs of the Test Board

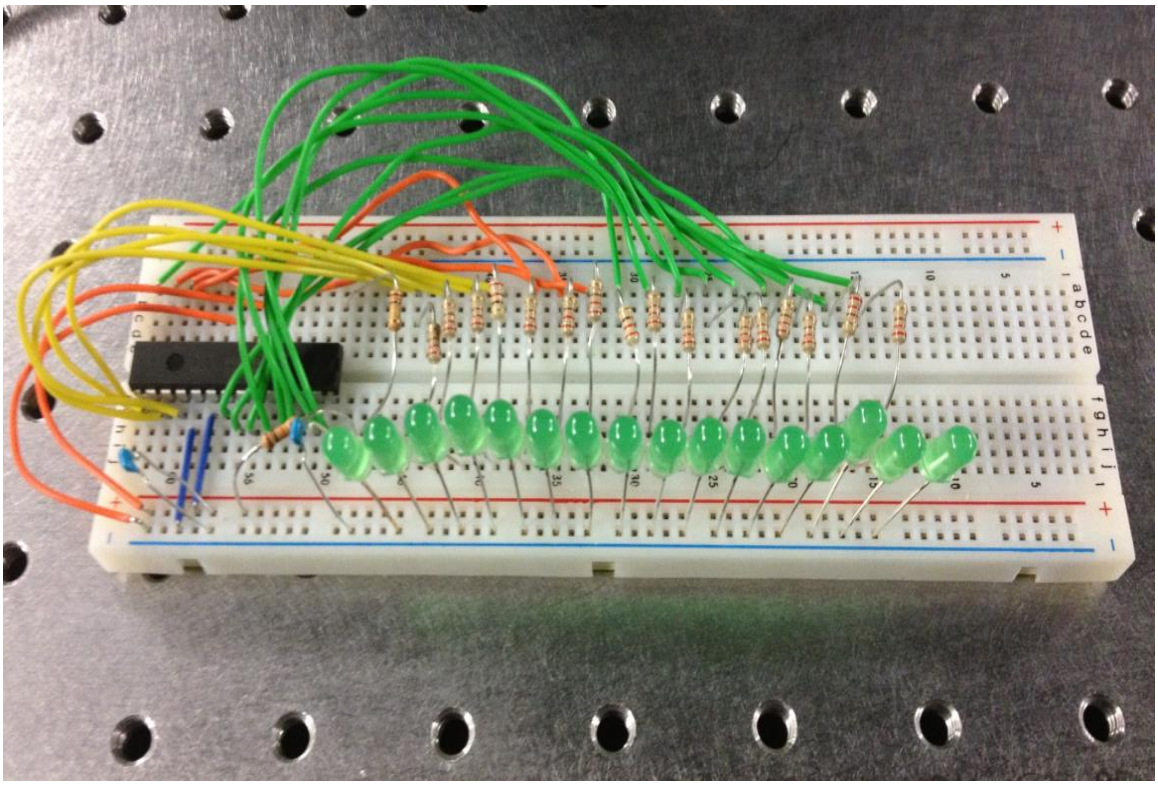


Figure 3.18: PIC Testing Breadboard

The programming of the PIC microcontroller was tested in a breadboard setup, shown above in Figure 3.18. The PIC microcontroller was programmed to use 16 different I/O pins to constantly cycle through each oscillation frequency. For this test setup, each I/O pin was connected to an LED to ensure that once connected to the oscillator IC, no two oscillators will be toggled on at the same time.

All output frequencies from the test board were measured using an Agilent N9320A Spectrum Analyzer while a GW Instek GPS-4303 power supply provided the necessary voltages.

Table 3.4: Measured Output Frequencies

Pin	Target Freq (MHz)	Measured Freq (MHz)
ctrl1	600	X
ctrl2	700	669.5*
ctrl3	800	X
ctrl4	900	X
ctrl5	1000	X
ctrl6	1100	X
ctrl7	1200	X
ctrl8	1300	1279
ctrl9	1400	1382
ctrl10	1500	1492
ctrl11	1600	1600
ctrl12	1700	1680
ctrl13	1800	1825
ctrl14	1900	1941
ctrl15	2000	2081
ctrl16	2100	2109

Table 3.4 shows the results as measured by the spectrum analyzer. Oscillators 1 and 3 through 7 did not function. The 700 MHz oscillator is marked with an asterisk because it was only observed to work intermittently. The primary reason for this failure is believed to be unintended currents not accounted for in the design of the circuit. There are four sources of this unintended current. First, turning off each oscillator by shorting the gate voltage of the current mirror was not an effective way of eliminating excess currents because the transmission gate "ON" impedance is not a perfect short circuit. The second source of unintended current comes from leakage coming from the output stage that is always on, regardless of whether or not the oscillator is on. Third, there is the feedthrough from the active oscillator output to the inactive oscillators, since no

transmission gate exists between each oscillator in the bank. Finally, the most significant source of error comes from the oscillator startup circuitry.

The startup circuitry that ties one oscillator output high and the other low does not account for the low series resistance of the inductor in the LC tank. The startup PMOS and NMOS transistors create a path from the supply rail to ground through the LC tank. This means that all of the "OFF" oscillators are actually drawing a considerable amount of current and some amount of energy storage on the LC tank is taking place.

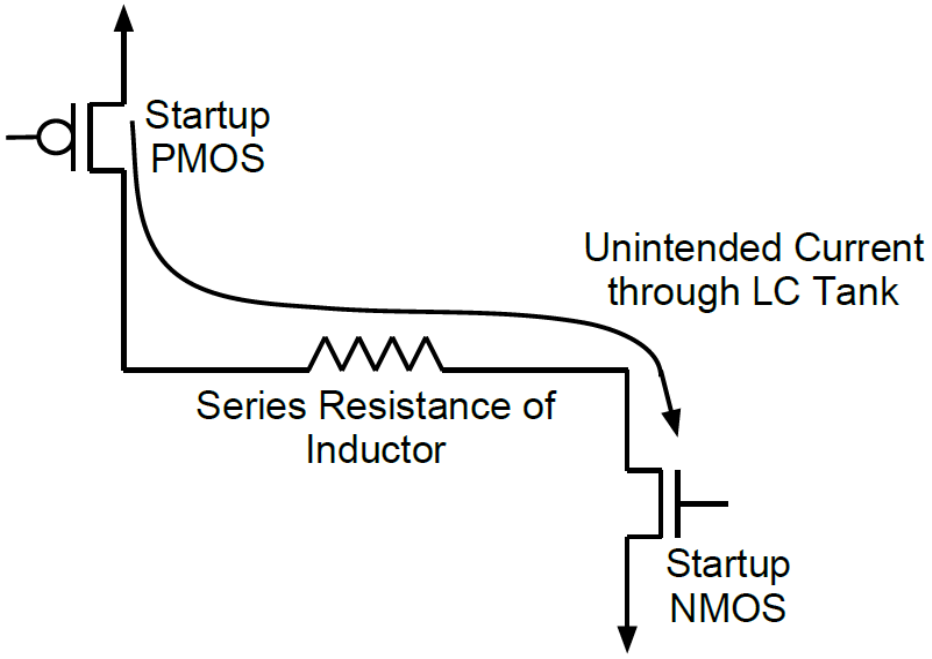


Figure 3.19: Startup Circuitry Current

These problems affected the lower frequency oscillators more because they have larger LC tanks, and are therefore more vulnerable to the stray currents and unexpected energy storage. These unintended DC currents combine to a total of 300mA of current draw by the final circuit, even with all of the oscillators in the "OFF" state. This amounts to 0.99W of wasted power being consumed. These issues are addressed in the voltage controlled oscillator bank design in Chapter 4.

Figure 3.20 shows a plot comparing the measured output oscillation frequency compared to both the simulated output and the intended frequency of the chirp. While the lower frequencies are not functioning reliably, the upper end of the range works with relatively good accuracy compared to the target frequencies. The measured results deviate from the target frequency the most with the 2 GHz oscillator, where 2.080 GHz was observed. While this is off by 80 MHz from the target, it is only 1 MHz different than the 2.081 GHz observed at simulation. This means that the final manufactured package tracked the simulated results very closely, and most of the error seen in the final measurements was also observed in the simulation results.

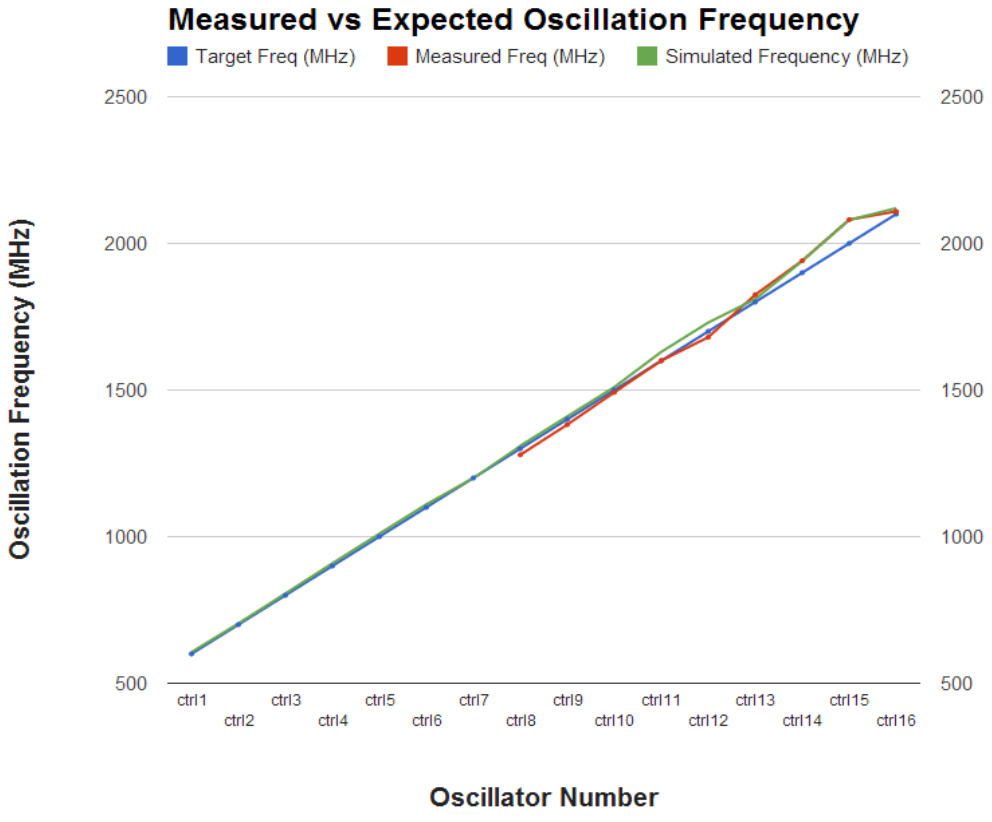


Figure 3.20: Measured Results Plot

Chapter 4

VOLTAGE CONTROLLED OSCILLATOR BANK (VCOB)

4.1 Chapter 4 Introduction

The purpose of this chapter is to describe the design, layout, and simulation of the voltage controlled oscillator bank chirp generator chip. This chapter is divided into five sections. First, an overall description of the capabilities and inputs and outputs of the chip are described in Section 4.2, as well as an overview of the shortcomings of the first chip that are addressed in the VCOB version. Next, Section 4.3 describes the design of each circuit block on the schematic level. Section 4.4 discusses the layout of each circuit block and post layout extraction, as well as other considerations related to the layout and packaging. Finally, Section 4.5 provides circuit simulation and verification.

4.2 VCOB Overview

The VCOB chirp generator IC is intended to both correct some of the mistakes made in the FFOB and also add additional functionality to the chip. First, the problem of excess currents being consumed by the circuit has been addressed. The method of deactivating "OFF" oscillators has been improved by using a transmission gate to cut off the power supply connection to the entire oscillator circuit, rather than just one branch of the current mirror. Additionally, there is only one output stage shared among all oscillators, further reducing current consumption. There are also transmission gates added to the output of each oscillator block to prevent one oscillator output from impacting another.

One of the design goals in the VCOB was to increase the number of frequency points from sixteen to thirty two. There is not enough space on the chip to have thirty two separate oscillators, so a new solution was needed. Varactors were utilized in each oscillator to provide a variable capacitance in the LC tank, so that each oscillator block is capable of generating a range of frequencies. This added functionality came with the drawback of needing to use smaller 1.8V transistors in the cross-coupled LC oscillator design so that the associated parasitics were small with respect to the varactor fine tuning. This resulted in a chip with lower overall current drive capability, having a peak-to-peak current drive of approximately 3 mA compared to about 30 mA in the previous chip. As having an amplification stage before driving the laser is an acceptable design requirement, this is not considered to be a significant drawback.

Another design goal was to be able to generate the digital control voltages that switch between each oscillator with on-chip circuitry. This was accomplished using a digital counter circuit that combined both an 8-bit counter and a 4-bit counter into one circuit block. These "counters" are not counters in the traditional sense of counting upwards in binary, but rather sequential synchronous bit shifters that count up by shifting a single logical high from one bit to the next, turning on each oscillator one at a time. This is implemented by having each continuous counter connected to the same clock signal, but one clock signal is delayed by consecutive frequency halving circuits. This ensures that the 4-bit counter cycles continuously through all four bits during each transition in the 8-bit counter.

Yet another advantage of the new design is the ability to tune the generator to create a continuum of frequencies, rather than just pre-set discrete values. This is possible by using an off-chip control voltage to bias the varactors in a custom setup. A near linear chirp signal could be obtained using a control signal matched to the varactor's capacitance-voltage characteristics.

The chip has a recommended control voltage configuration that utilizes two supply voltages of 3.3V and 1.8V, as well as four other inputs to control the varactor biasing of 1.1V, 1.5V, 2.2V, and 3.2V. This configuration will result in a 32-step chirp using just 8 oscillators (four discrete frequencies per oscillator) with a chirp frequency determined by on off chip clock. The varactor control voltages may be changed to meet the application, as can the clock frequency, but the following documentation assumes that the chip is biased with the four voltages provided above. A block diagram of the inputs and outputs is provided below in Figure 4.1.

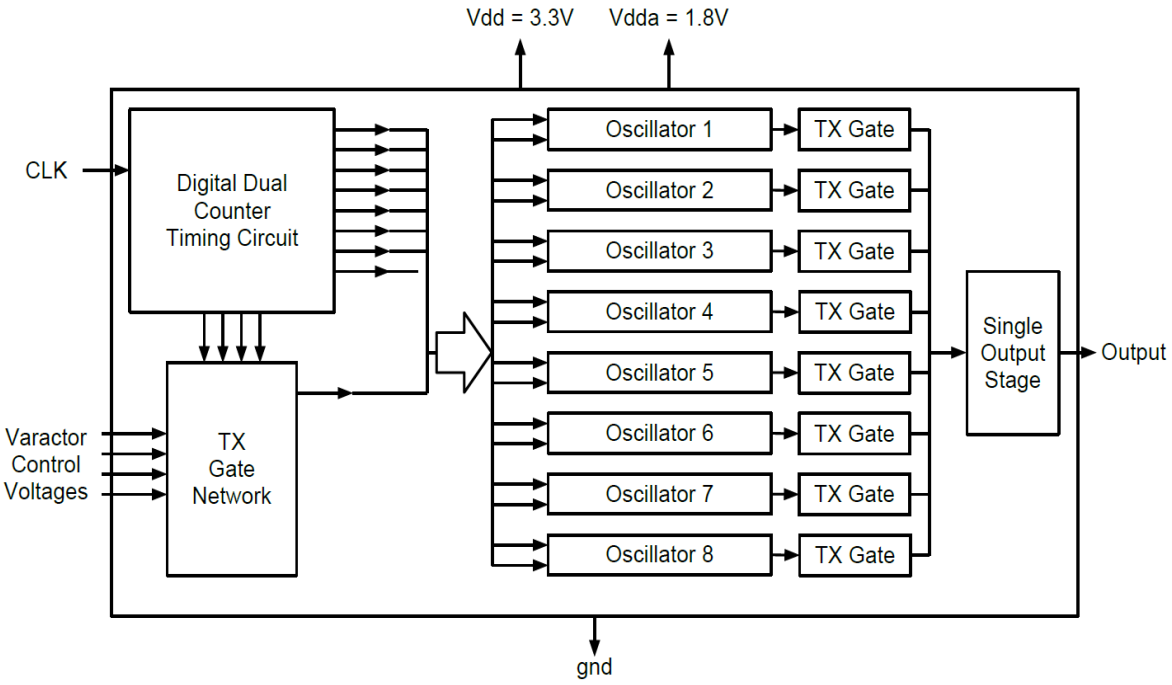


Figure 4.1: The VCOB Chip

A dual power supply is used, and inputs include four varactor control voltages and a single clock. The transmission gate network and the dual counter timing circuit ensure that each of the eight oscillators has the necessary inputs to generate a total of 32 frequencies that are all tied to a single chip output pin.

4.3 Design and Schematics

The design of each individual circuit block of the VCOB are each described in the following subsections, which schematics and descriptions of how each circuit block interacts provided.

4.3.1 The Dual Counter

The purpose of the dual counter is to provide the signals necessary to turn on each of the oscillators one at a time in sequence, and also to control the transmission gate network to send the correct off-chip varactor bias voltage to the active oscillator. This dual counter has a single clock input and 12 digital outputs and operates on a 3.3V supply.

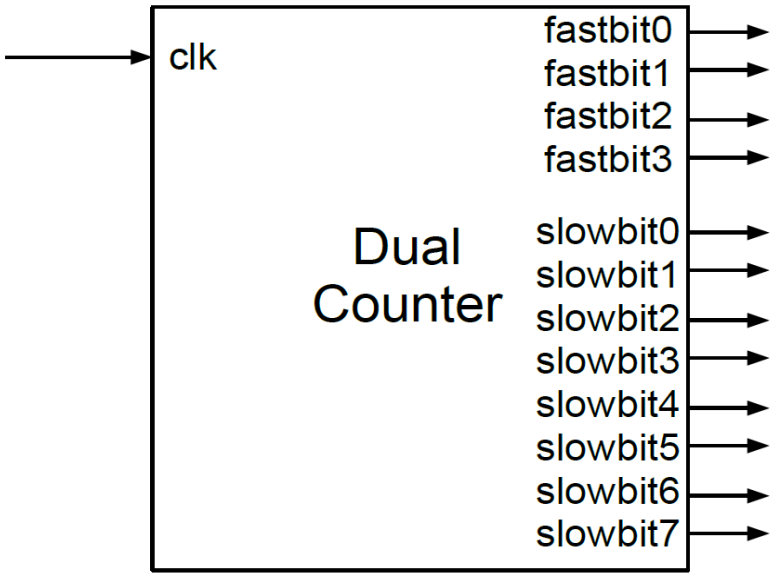


Figure 4.2: The Dual Counter Symbol

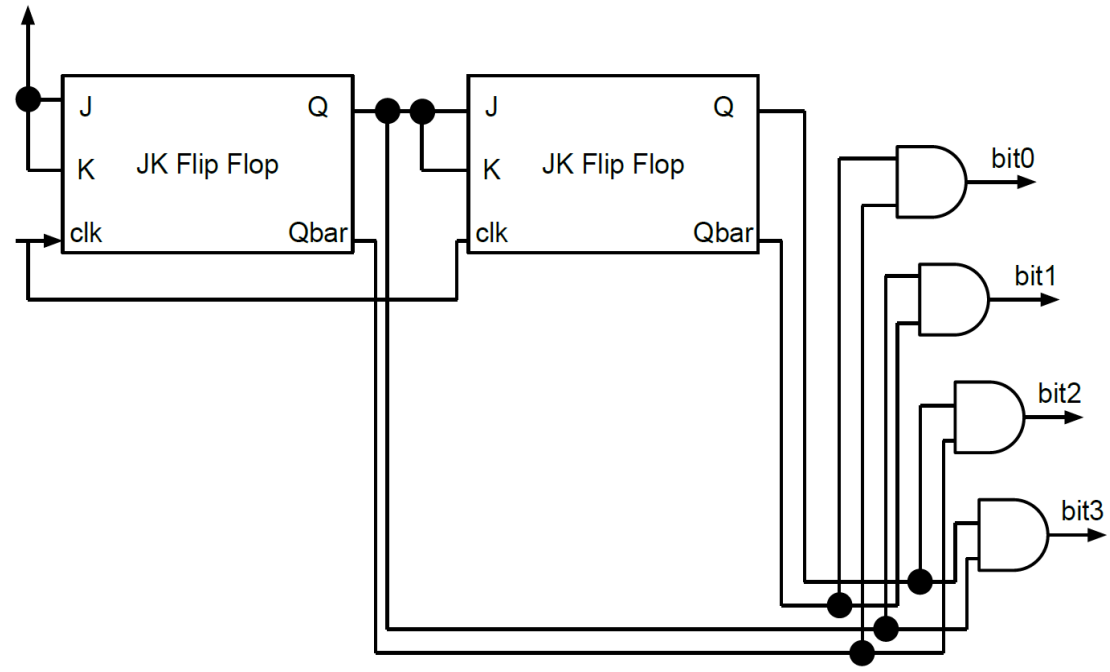
Four of the dual counter's outputs are called "fast bits." These are digital signals that operate at one half of the input clock frequency and each one turns on and off sequentially. These digital bits are used to control the transmission gate network that selects which of the four varactor bias voltages to apply to the active oscillator block.

The other eight outputs are called "slow bits." These are digital signals that operate at one quarter of the frequency of the fast bits and each bit toggles on and off sequentially in the same manner as the fast bits. Their purpose is to select which of the eight oscillator blocks is active while all others are inactive.

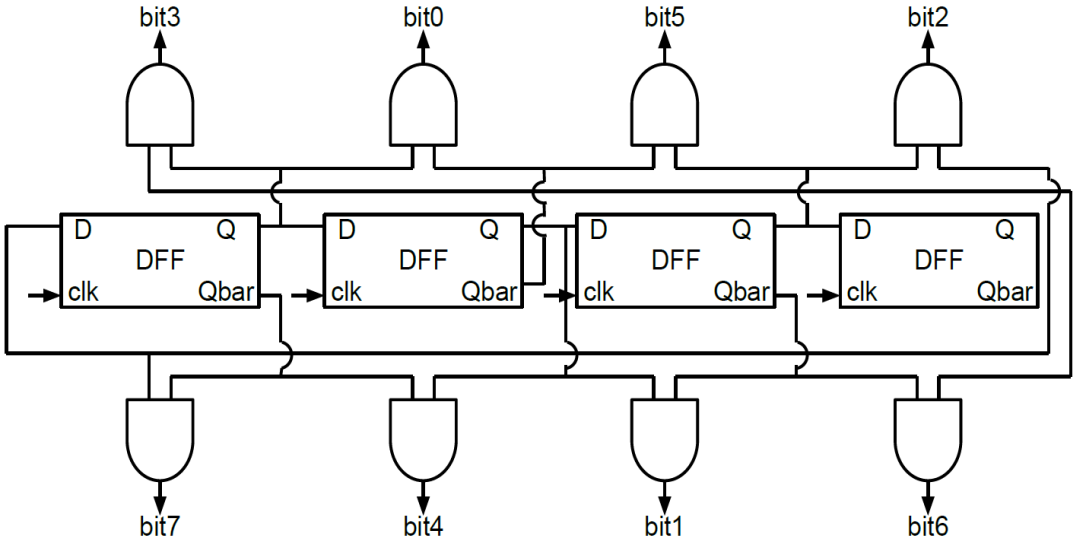
By combining both a 4-bit digital counter and an 8-bit digital counter, the dual counter provides a system wherein a slow bit will turn on the first oscillator, then cycle through all four varactor bias voltages, then turn on the next oscillator and again cycle through all four varactor bias voltages. This system repeats indefinitely to generate the thirty two step chirp signal, where four different frequencies are output from each of the eight oscillator blocks. Both the 8-bit and 4-bit counters operate from the same clock input, except the 8-bit counter's clock signal is first halved twice using flip flops in order to create the desired timing scheme.

The upper limit on the clock frequency is 500 MHz. This results in a fast bit period of 4 ns, and an overall chirp period of 128 ns. Therefore the minimum chirp period provided by the dual counter is 128 ns, but can be as long as desired by the user.

The schematic drawing for the 4-bit counter is shown in Figure 4.3a, while 4.3b shows the 8-bit counter.



(a)



(b)

Figure 4.3: 4-bit and 8-bit Counter Schematics

The counter topology shown in each of the schematics in Figure 4.3 are common shift register ring counter circuits utilizing flip flops to toggle digital signals while logical AND gates are used to decode the outputs of the flip flops to extract the desired sequential digital outputs [9]. The design of these blocks are not novel and the in-depth analysis of their functionality is not within the scope of this thesis. The relevant schematics used are provided in this section, however, and the layout and simulation verification of their operation are provided in the sections to follow. The schematic drawing of the logical AND gate used in these blocks is provided below in Figure 4.4, with device sizing based on a unit inverter.

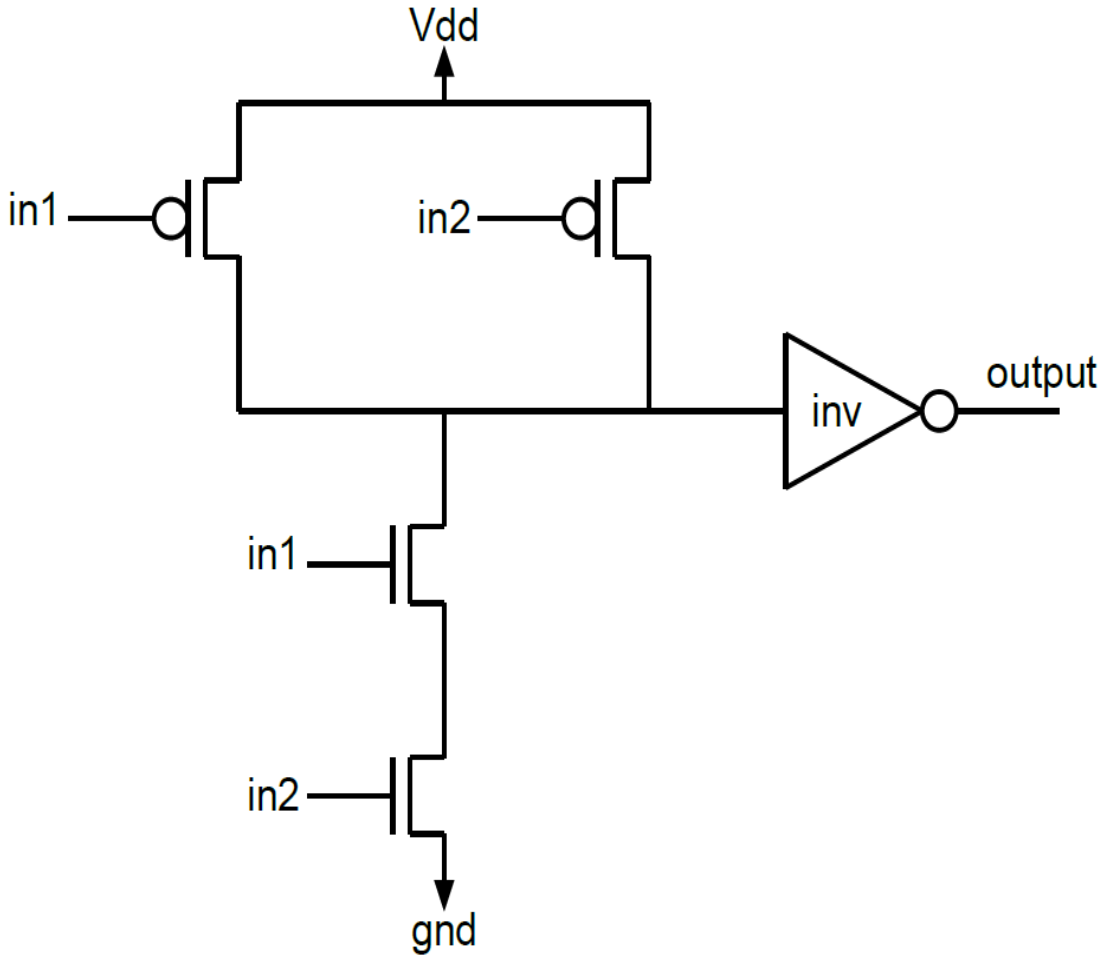
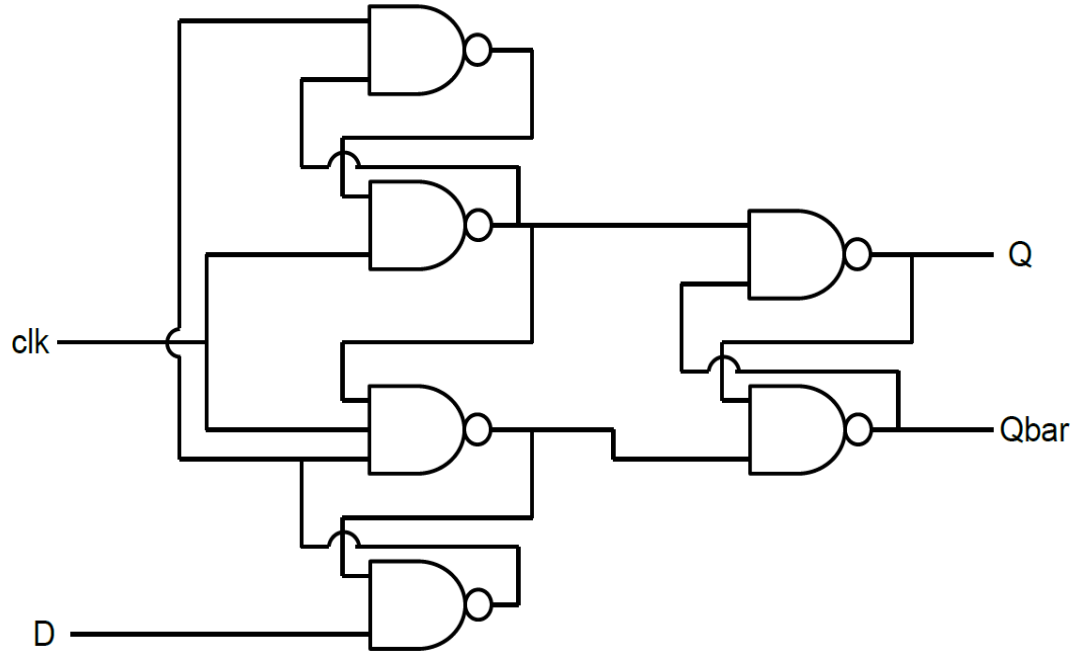
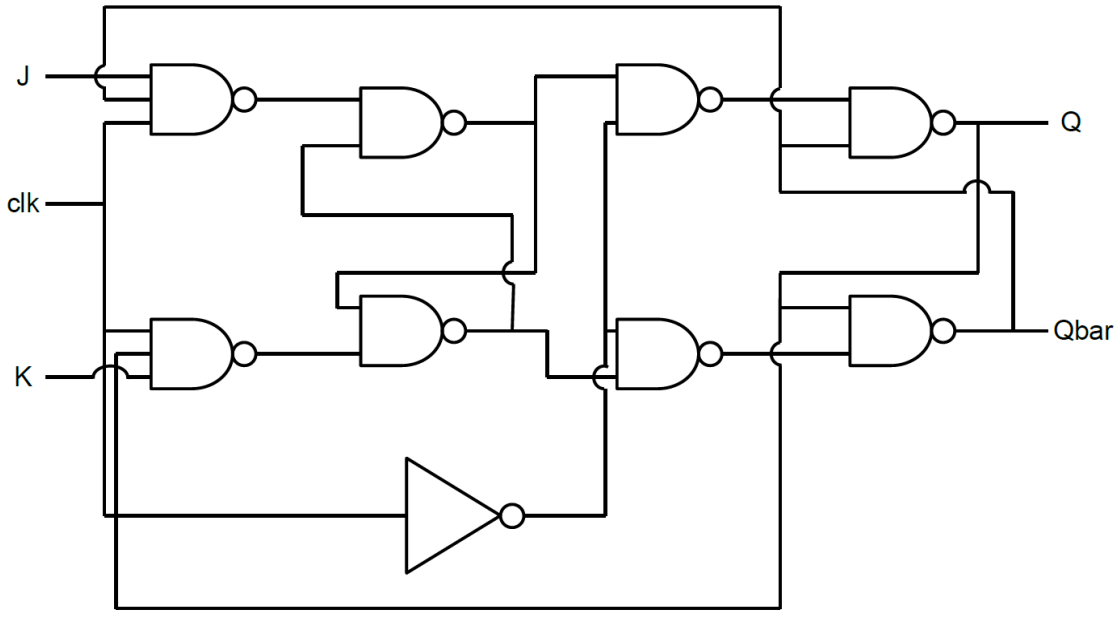


Figure 4.4: AND Gate Schematic

The schematics for both the JK flip flop and positive edge triggered D flip flop are provided below in Figures 4.5a and 4.5b, respectively.



(a)



(b)

Figure 4.5: Flip Flop Schematics

4.3.2 The Voltage Controlled Oscillator

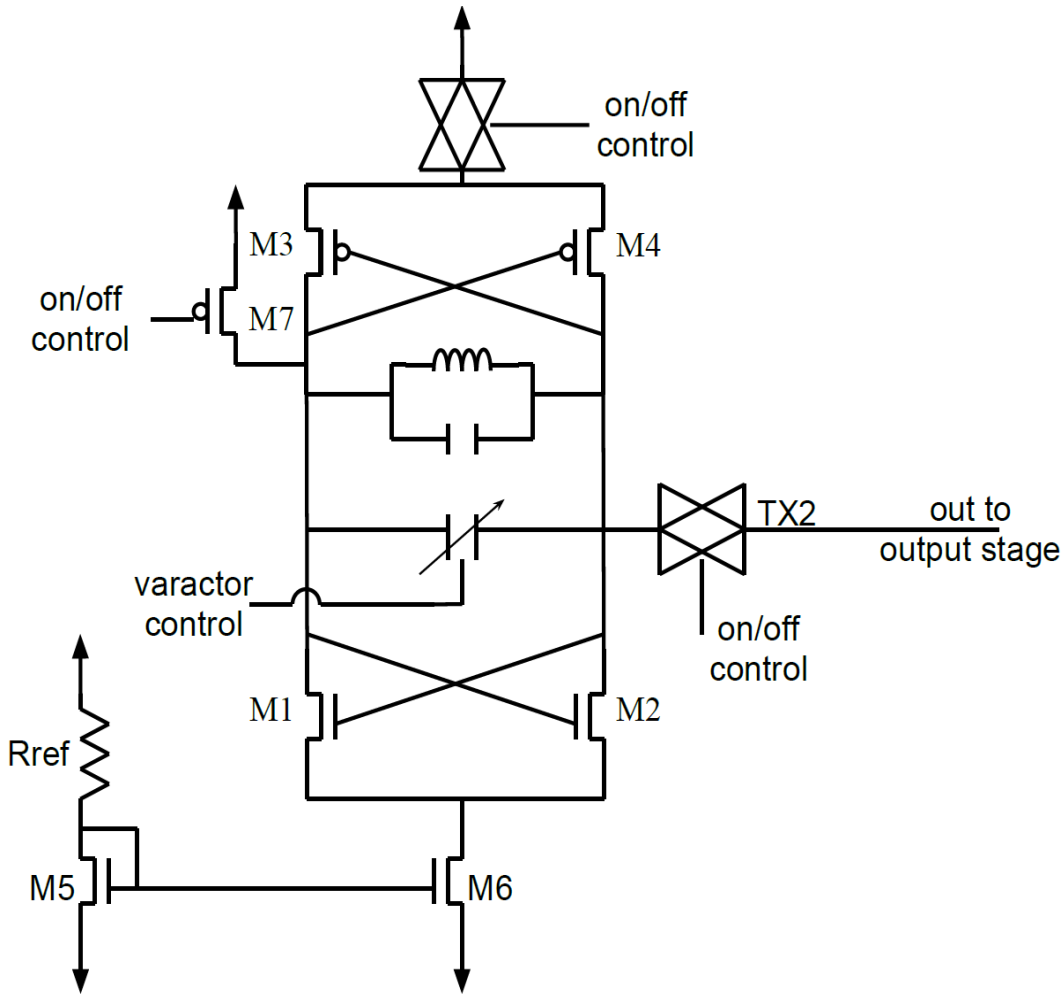


Figure 4.6: The New Oscillator Schematic

The schematic for one oscillator used in the VCOB design is provided above in Figure 4.6. In this design, a transmission gate is used to disconnect the oscillator from the 1.8V supply voltage, resulting in a significant current reduction compared to the FFOB design. Additionally, there is a second transmission gate added to the output of the oscillator to prevent unintended currents from interfering with other oscillator outputs. The transistors used in this oscillator design are the smaller 1.8V devices compared to the 3.3V devices used in the FFOB design.

The key difference between this oscillator and the FFOB oscillator is the varactor, which allows the oscillation frequency to be tuned with a control voltage. The LC tank consists of one inductor, one fixed capacitance, and one variable capacitance provided by the varactor. The varactor model offered in the IBM CMRF7SF process is a scalable varactor diode that is a P+/N junction diode, where the P+ region is similar to the PFET source and drain and the N region is composed of N+ subcollector and a specially tailored N-type spike to enhance tunability and lower series resistance.

The nominal value equation for the capacitance of the varactor is provided by the CMRF7SF design manual as

$$C_{Nom}(V) = (C_A(V) \cdot L \cdot W \cdot N) + (C_P(V) \cdot 2N \cdot (W + L)) \quad (4.1)$$

where C_{NOM} is the nominal capacitance in Farads, $C_A(V)$ is the capacitance per area, L us the device length, W is the device width, N is the number of anodes, and $C_P(V)$ is the capacitance per length.

By adjusting the device sizes of both the fixed capacitor and the varactor in each oscillator circuit, a linearly increasing set of thirty two discrete oscillation frequencies is achieved in the recommended configuration.

Another notable change in this design is the removal of the NMOS pull-down transistor used in the startup circuitry. By relying on only the PMOS pull-up on the opposite output, a current path is not established in the “OFF” state through the equivalent series resistance of the LC tank. This drastically reduces the stray current draw seen in the FFOB chip, thus cutting back on power consumption.

4.3.3 The Output Stage

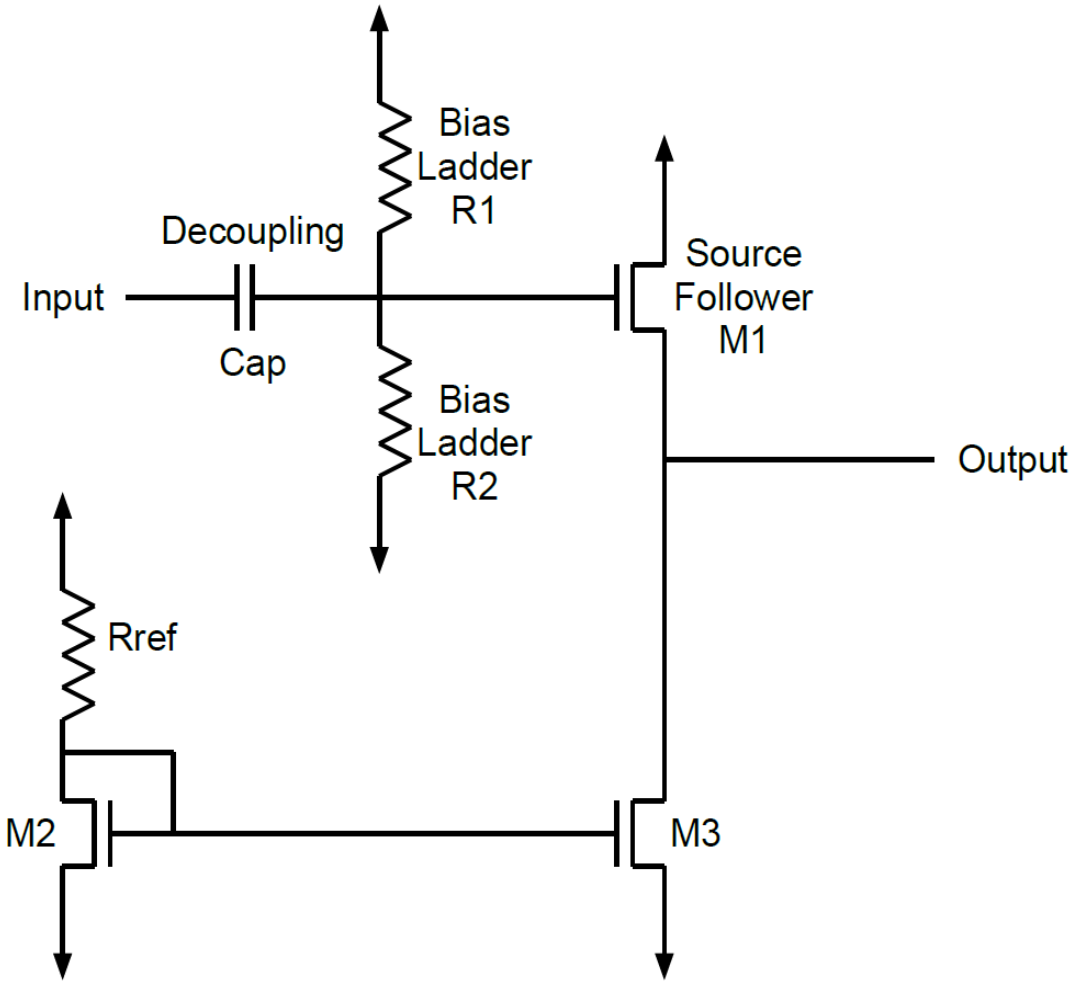


Figure 4.7: Output Stage Schematic

The schematic drawing for the single output stage is provided above in Figure 4.7. The output stage is once again a single source follower NMOS stage designed to increase the current drive capability of the circuit to a 50 Ohm load, however a number of improvements have been made. First, there is only one output stage, so less current is wasted generating seven unnecessary reference currents, unlike the first chip. Second, a

decoupling capacitor and resistor ladder is used to ensure that the input to the source follower is completely within its linear compliance range, reducing distortion compared to the previous chip.

4.3.4 Complete Schematic

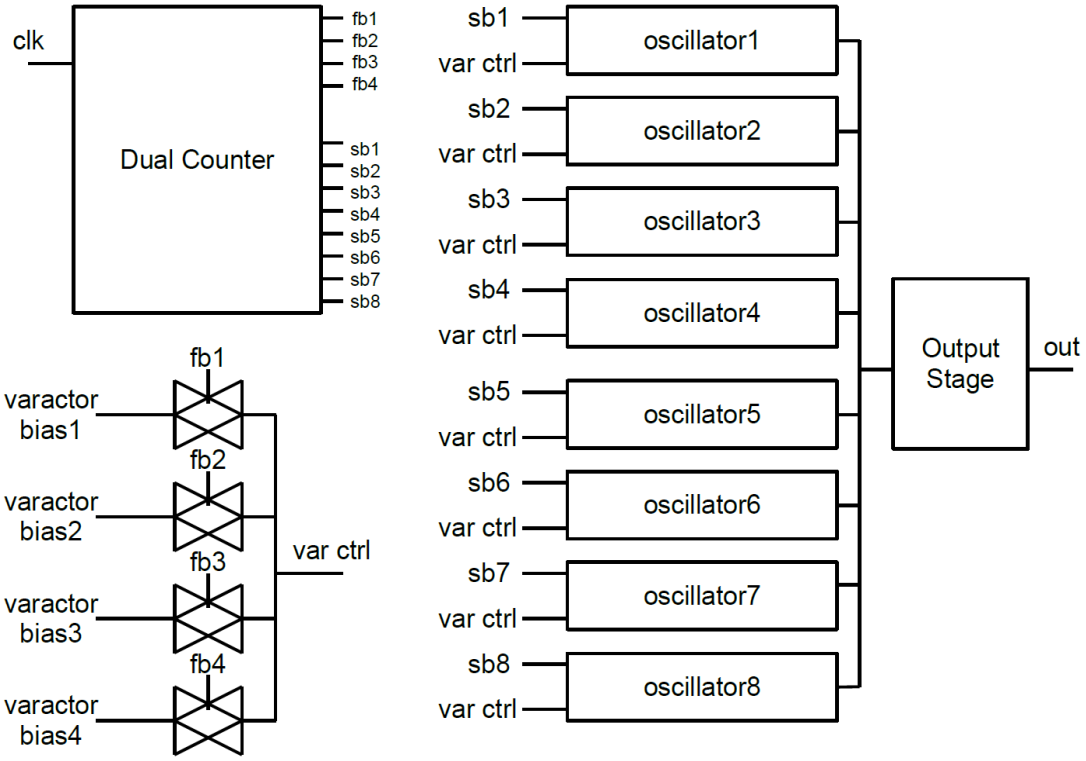


Figure 4.8: The Complete VCOB Schematic

The final schematic including all circuit blocks is shown in Figure 4.8. The dual counter provides the digital signals necessary to control both the transmission gates and select the active oscillator and 32 discrete frequencies are output on a single pin, as described in Section 4.3. The following section will provide layout views as well as packaging information.

4.4 Layout and Packaging

The following subsections describe the layout of each of the major circuit blocks in the second chip revision.

4.4.1 The Dual Counter Layout

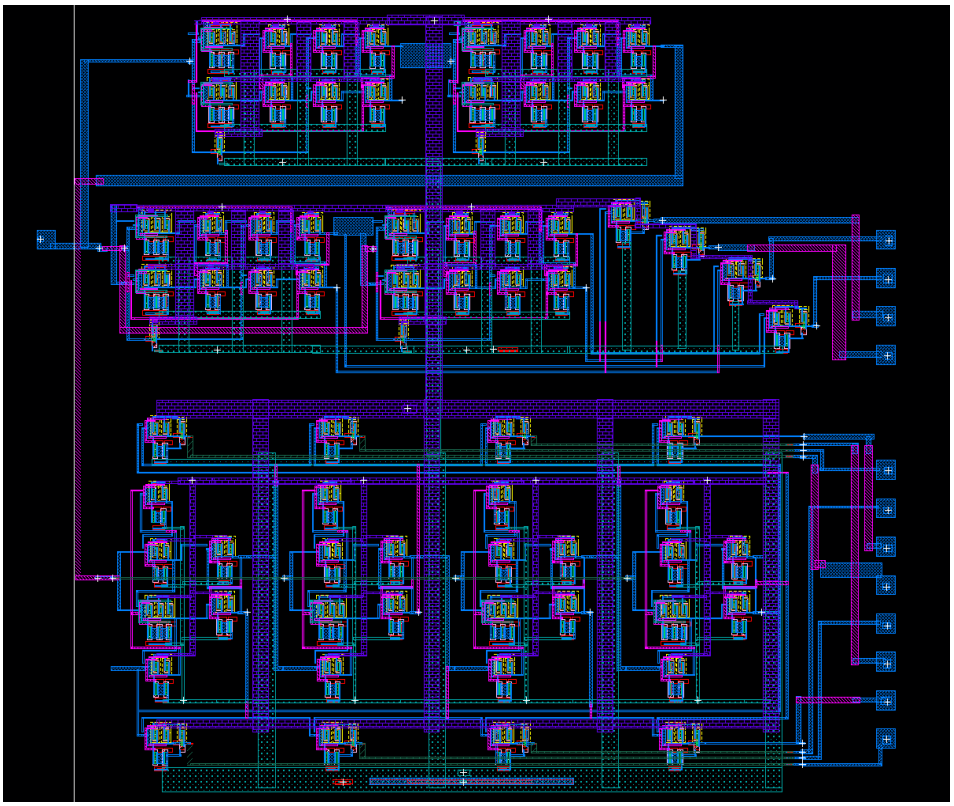


Figure 4.9: Dual Counter Layout

The dual counter layout is made up of mostly AND gates and flip flops. Wiring does not require wide metal lines compared to the FFOB because there is a very low current draw from this block of the circuit, as its outputs only feed the gate terminals of the transmission gates and oscillators. The 8-bit counter occupies a 195µm by 100µm area, while the 4-bit counter occupies a 195µm by 45µm area. The rest of the total 200µm by 230µm area is taken up by the frequency halving circuitry and wiring.

4.4.2 Transmission Gate Layout

The layout of the transmission gate is very similar to the one found in Chapter 3, as very few changes have been made to the circuit. The transistors used are smaller, as are the metal wire connections, as the currents used in this version of the chip are lower (2mA maximum compared to 30mA) in comparison to the first iteration. The overall transmission gate in the VCOB design occupies a 30µm by 18µm area, whereas the FFOB transmission gate occupied 55µm by 30µm.

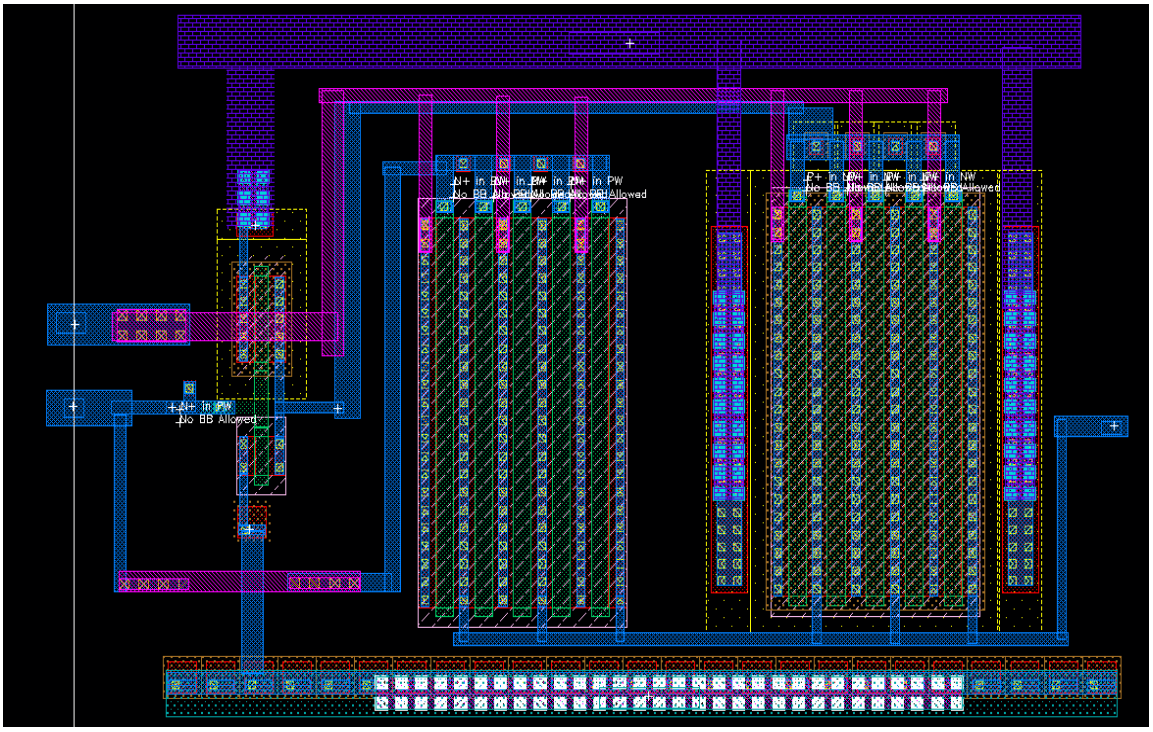


Figure 4.10: Transmission Gate Layout

4.4.3 The VCOB Oscillator Layout

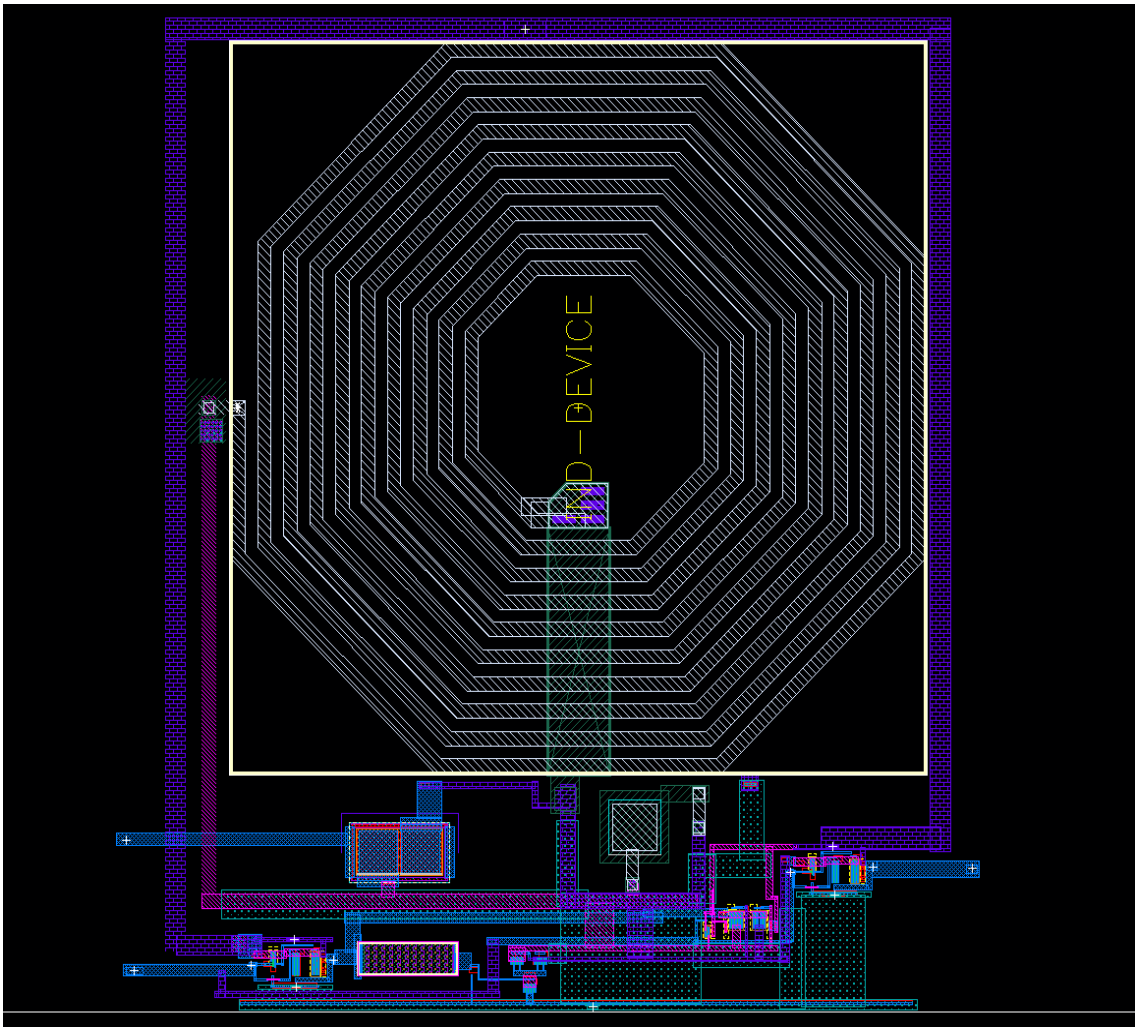


Figure 4.11: The New Oscillator Layout

The oscillator in this chip design was considerably easier to layout than the FFOB design, as the currents are less than one tenth of what was found in the previous chip. More space was also available since there is not an output stage associated with every single oscillator block. This entire block occupies 190µm by 225µm, compared to a 200µm by 270µm area occupied by the FFOB oscillator design.

4.4.4 Output Stage Layout

The layout of the output stage is provided below. The entire block occupies an area that is 95µm by 40µm, with a 25µm square being taken by the 1pF decoupling cap. The source follower NMOS occupies 28µm by 10µm.

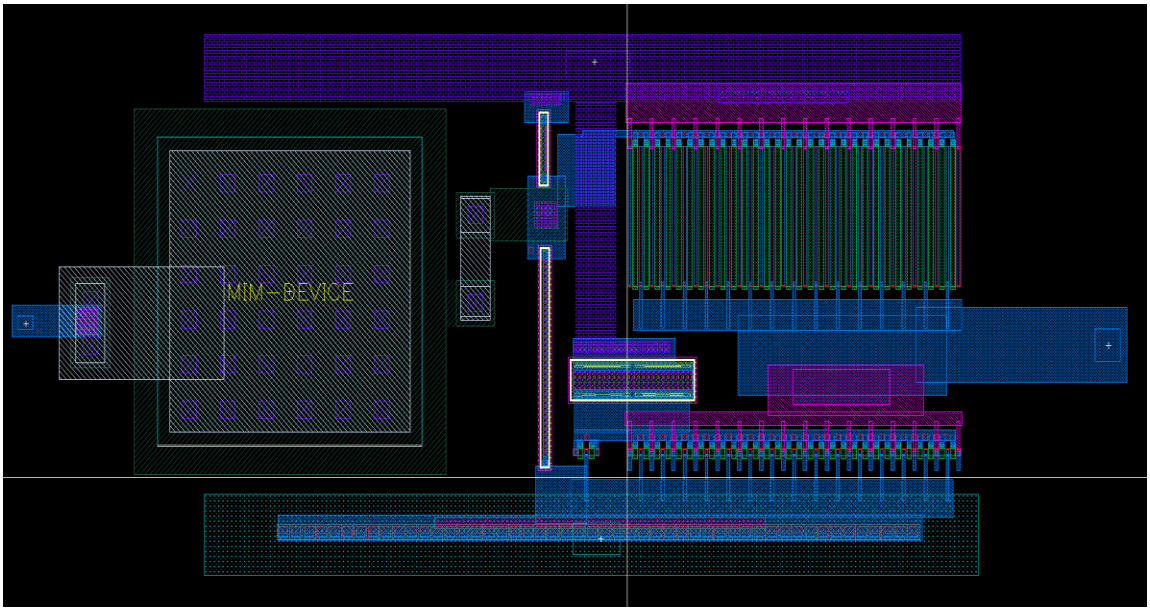


Figure 4.12: The Output Stage Layout

4.4.5 The Complete VCOB Layout

The layout of the entire second revision chip is provided in Figure 4.13. It occupies the same 1500µm square as the first chip. This layout includes eight oscillators and a dual counter circuit, as well as an additional oscillator and dual counter for testing purposes.

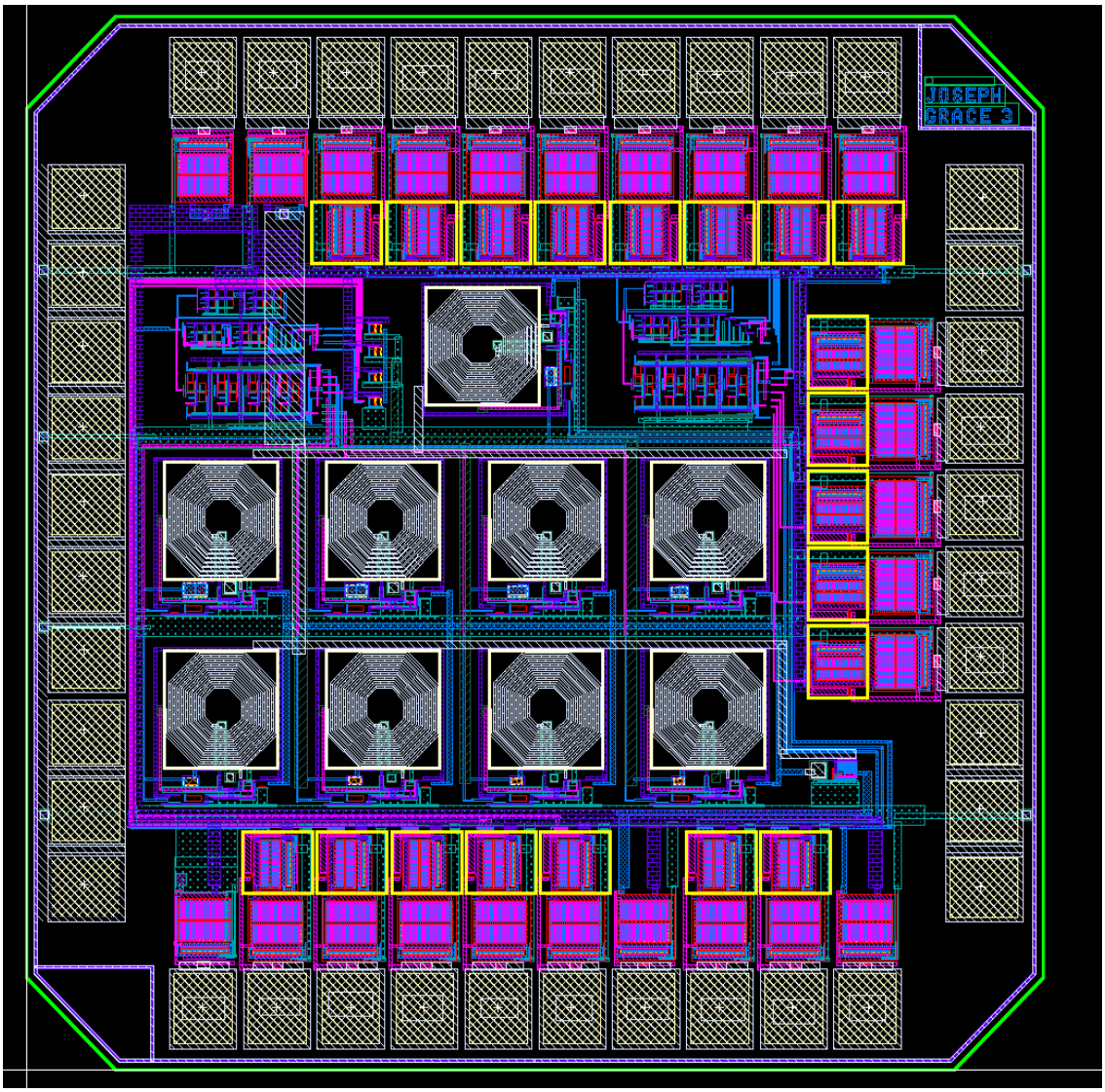


Figure 4.13: Compete VCOB Layout

This layout uses the same ESD devices as the first iteration, but does not place them below the package pads. This is because with eight less oscillator cells required, space is less of a concern. Additionally, this makes the layout far more easy to read and alter without intimate knowledge of the design.

The layout also includes an extra oscillator and dual counter with all of their inputs and outputs tied directly to package pins for the purposes of device testing and troubleshooting. A symbol of the entire package is shown below.

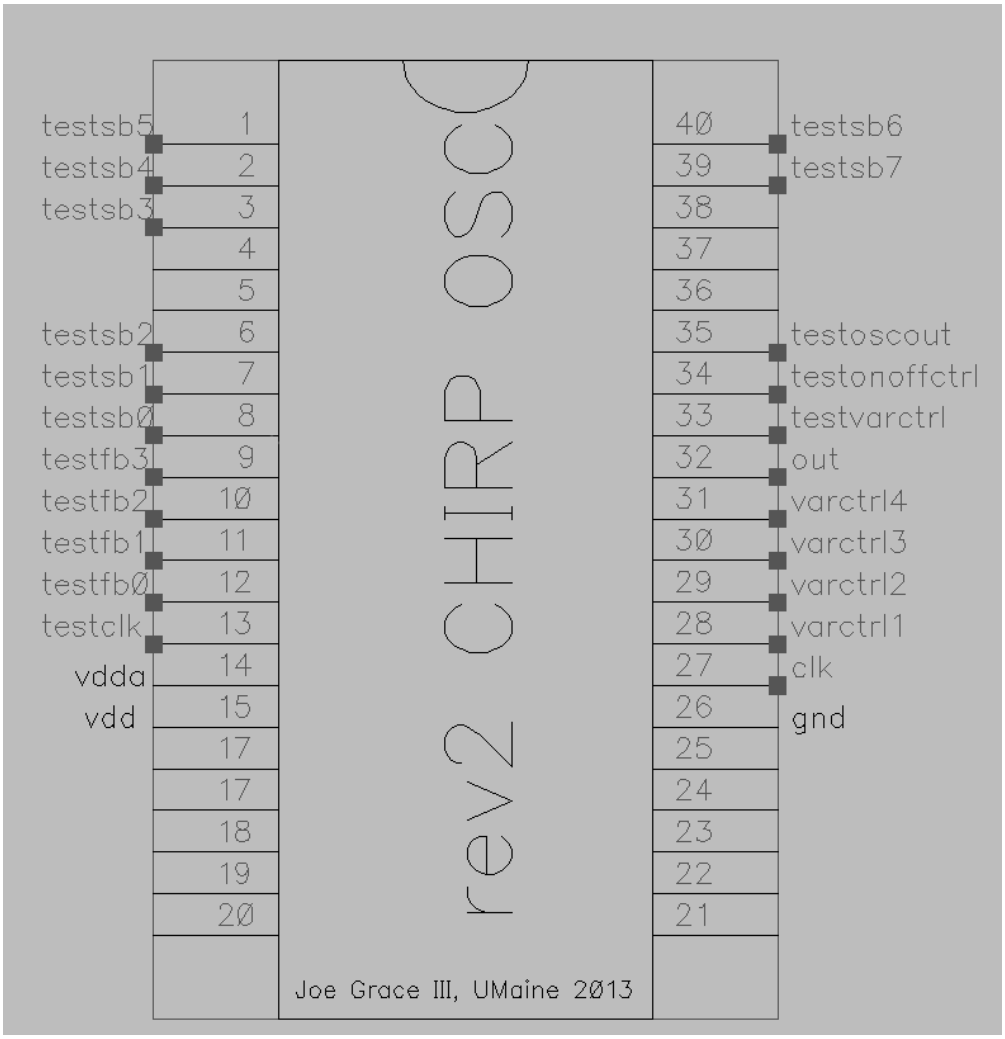


Figure 4.14: Package Symbol

Just as in the FFOB, each package pin has an associated set of parasitic components associated with it as described by the package handbook provided by MOSIS. Information on these package parasitics is provided in Table 4.1.

Table 4.1: Package Parasitics

Pin Num	Usage	R (ohms)	L (nH)	C (pF)
1	testcounterslowbit5	0.217	8.18	5.32
2	testcounterslowbit4	0.177	7.92	4.39
3	testcounterslowbit3	0.154	7.34	3.37
6	testcounterslowbit2	0.0661	4.37	1.43
7	testcounterslowbit1	0.0646	4.54	1.48
8	testcounterslowbit0	0.0498	3.69	1.05
9	testcounterfastbit3	0.0378	3.54	0.863
10	testcounterfastbit2	0.0247	3.15	0.66
11	testcounterfastbit1	0.0247	3.15	0.66
12	testcounterfastbit0	0.0378	3.54	0.863
13	testcounterclk	0.0498	3.69	1.05
14	vdda	0.0646	4.54	1.48
15	vdd	0.0661	4.37	1.43
26	gnd	0.0661	4.37	1.43
27	clk	0.0646	4.54	1.48
28	varctrl1	0.0498	3.69	1.05
29	varctrl2	0.0378	3.54	0.863
30	varctrl3	0.0247	3.15	0.66
31	varctrl4	0.0247	3.15	0.66
32	out	0.0378	3.54	0.863
33	testoscvarctrl	0.0498	3.69	1.05
34	testosconoffcontrol	0.0646	4.54	1.48
35	testoscout	0.0661	4.37	1.43
39	testcounterslowbit7	0.177	7.92	4.39
40	testcounterslowbit6	0.217	8.18	5.32

4.5 Simulation and Verification

This section provides simulation plots that verify the operation of the device. The VCOB chip has not been manufactured as a part of this thesis work, and these simulations represent the verification completed on the chip. This chip features a power consumption of less than 18 mW while active, a dramatic reduction from the 990 mW of power consumed by the FFOB.

4.5.1 Dual Counter Simulation and Verification

The dual counter's so-called "fast bits" are shown in Figure 4.15 as part of a transient simulation, shown below the clock signal input. One turns on after another sequentially, as desired. Additionally, each bit is on for exactly one full clock period.

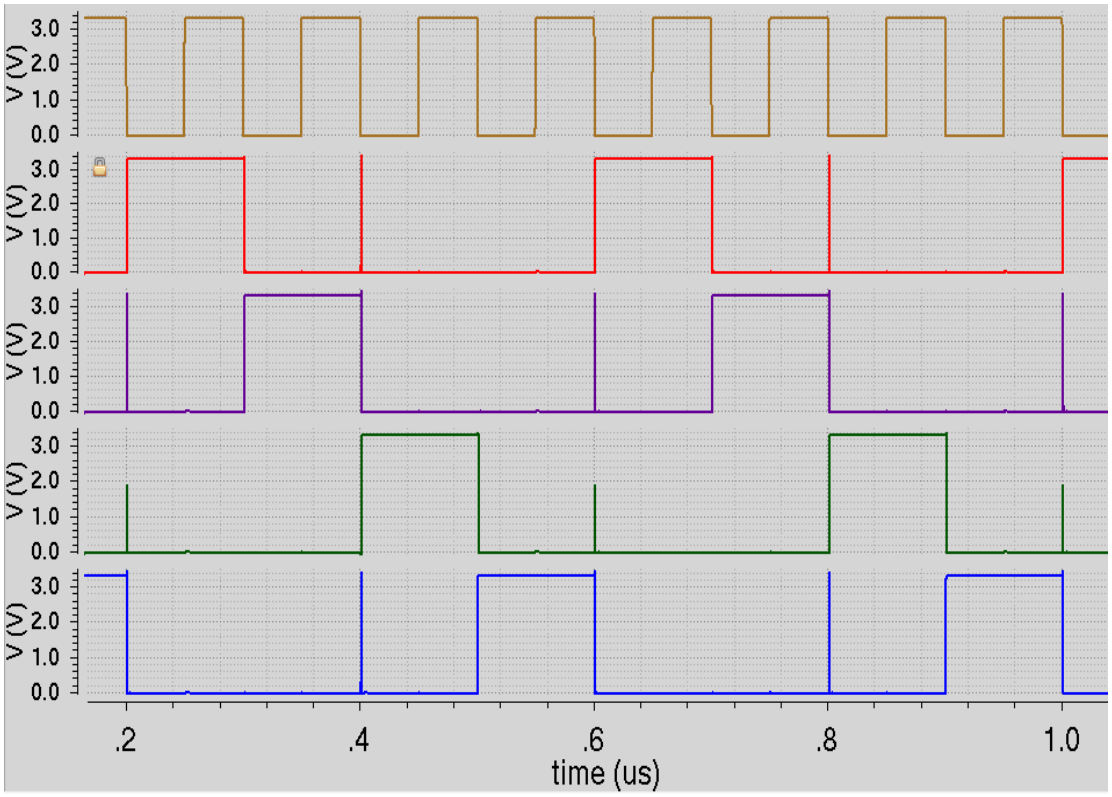


Figure 4.15: Dual Counter Fast Bits Simulation

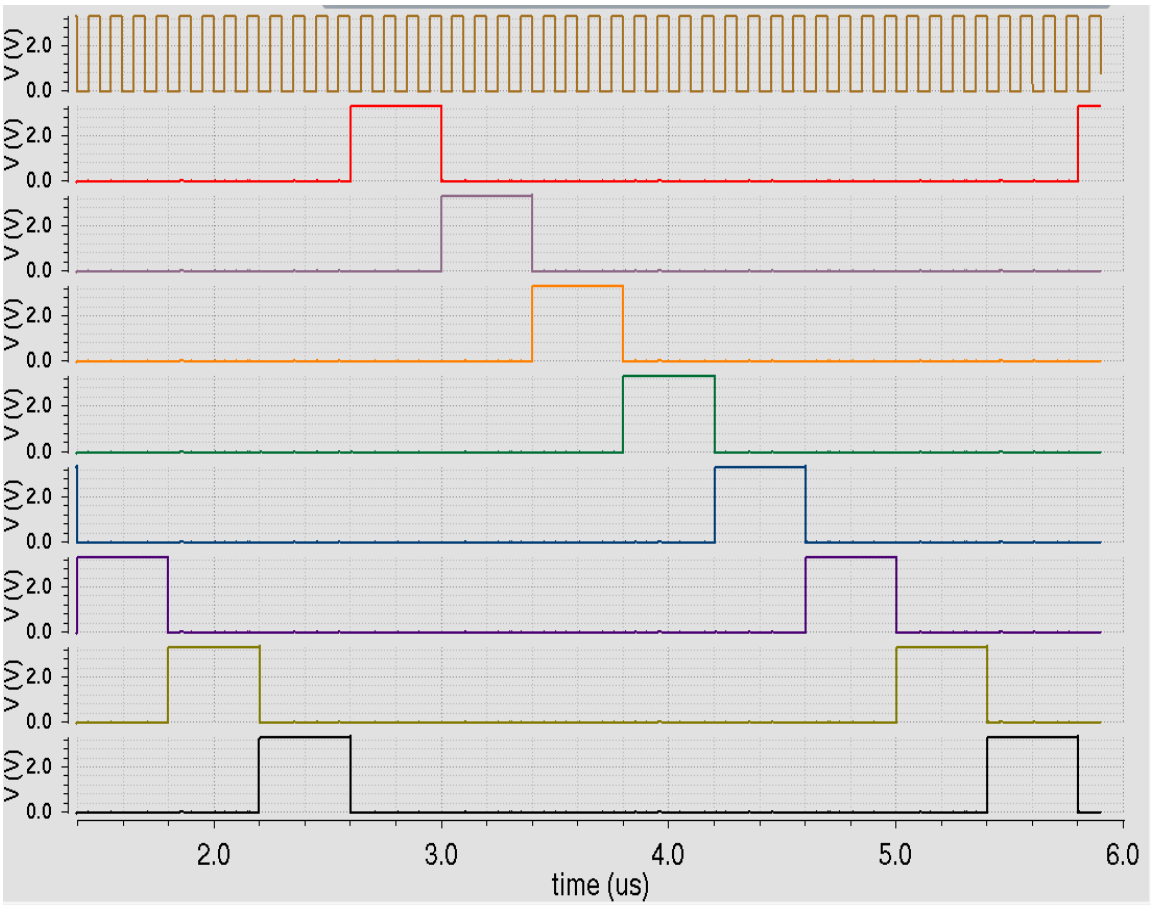


Figure 4.16: Dual Counter Slow Bits Simulation

Figure 4.16 shows the first five slow bits in comparison to the same clock signal. Each bit turns on sequentially, as desired. Each bit pulse is the duration of four full clock periods, which allows each fast bit to be toggled sequentially during each slow bit pulse. This is what allows each of the eight oscillators to be operated with four different varactor bias voltages sequentially.

4.5.2 Oscillator Simulation and Verification

The FFOB oscillator showed significant peaks in the frequency domain at multiples of the target frequency and also near DC component due to the nonlinearity of the oscillator output. Figure 4.17 shows that all of the improvements made in the VCOB design have dramatically reduced the magnitude of the 2nd harmonic distortion and also eliminated the low frequency peak seen in the FFOB design. This plot shows the output current of the system driving a 50 Ohm load with a decoupling capacitor.

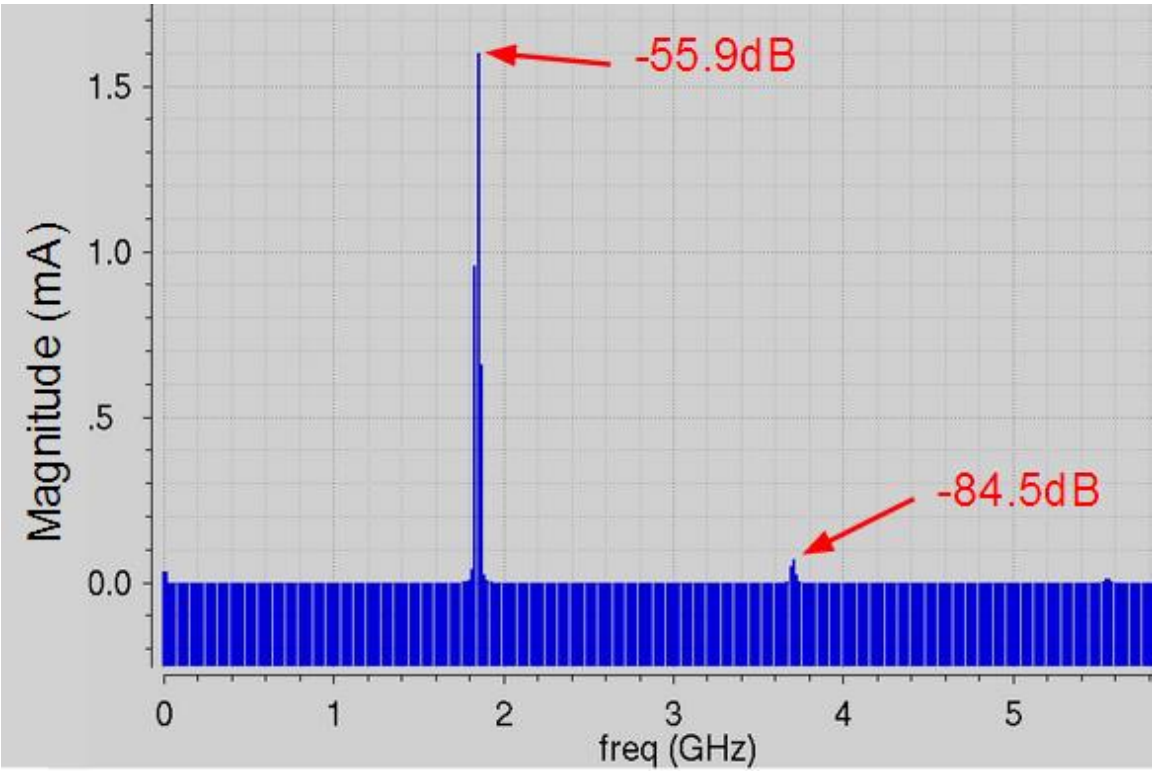


Figure 4.17: The New 1.85 GHz Oscillator Frequency Domain Simulation

This translates to a much cleaner sinusoidal waveform output when examined in transient simulation, as shown below in Figure 4.18. Unlike the FFOB design simulation, there are no signs of distortion as the sinusoid appears strongly symmetrical.

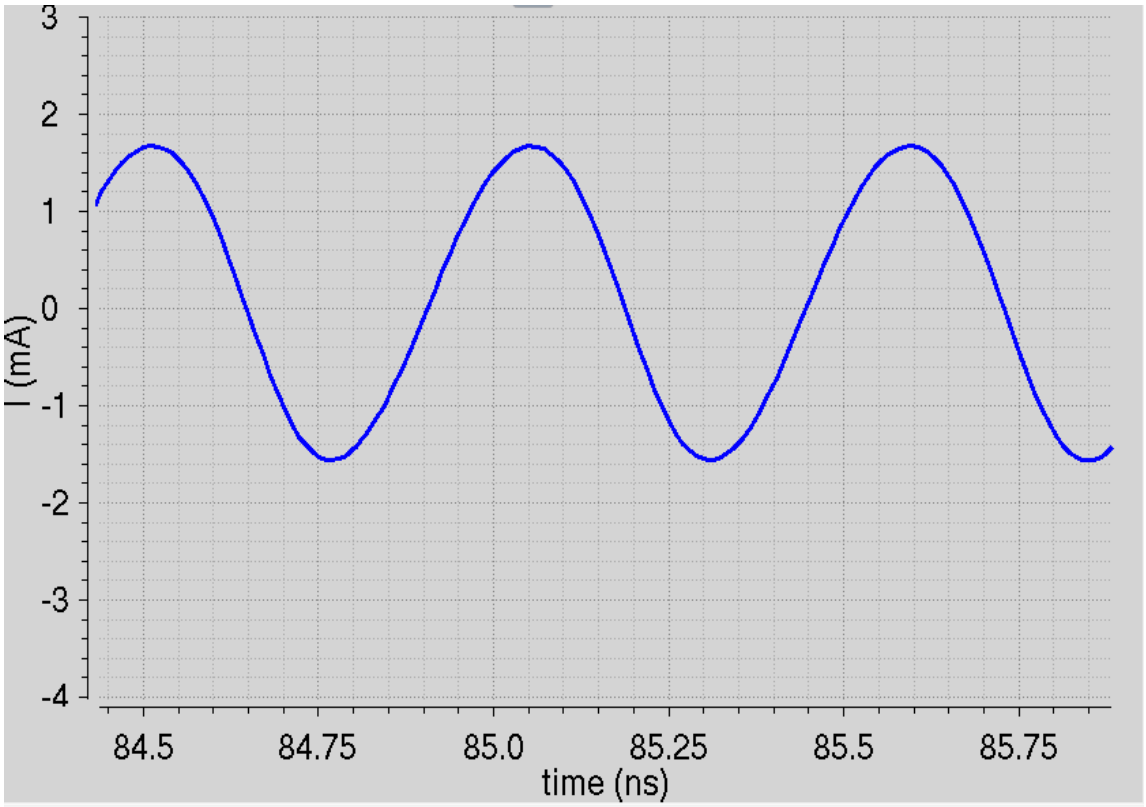


Figure 4.18: Transient Simulation of VCOB 1.85 GHz Oscillator

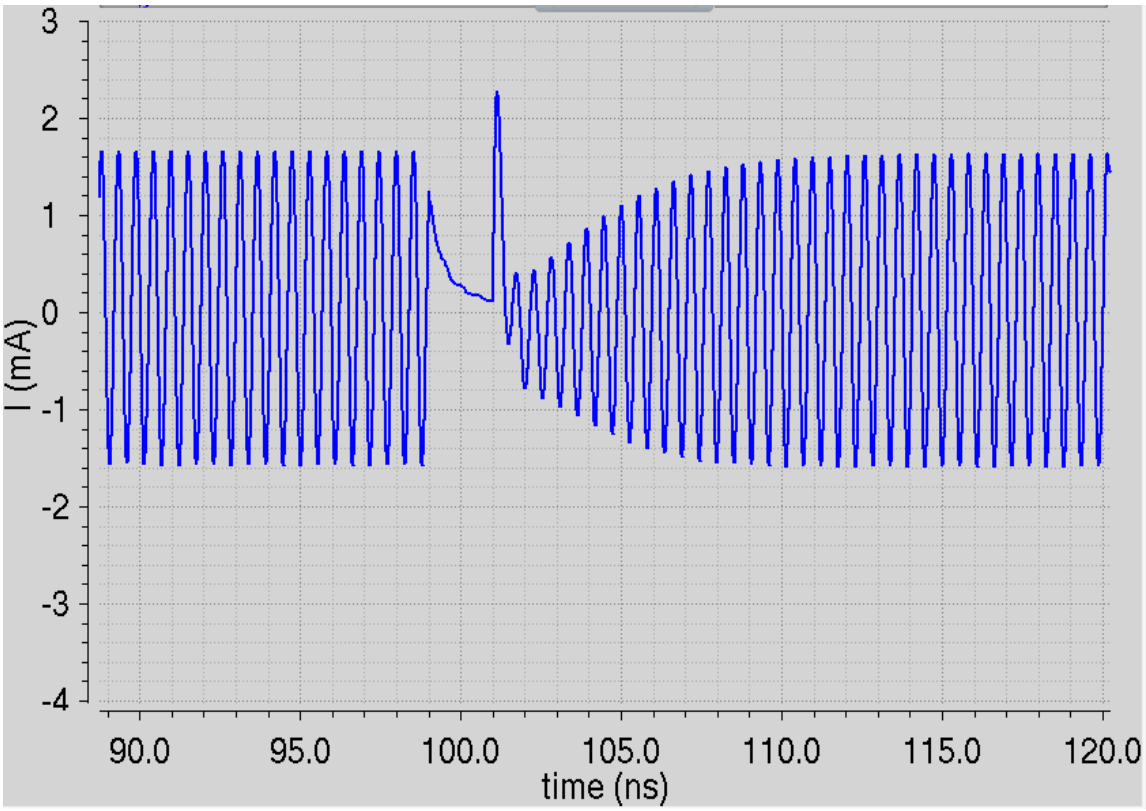


Figure 4.19: VCOB Oscillator Transition Simulation

Figure 4.19 demonstrates the clean transitions from one oscillator to the next as controlled by the dual counter. It takes approximately 12 to 15 ns to stabilize at the new frequency, so chirp periods that rely on times shorter than about 50 ns per frequency are not advised. The output amplitude is more uniform compared to the FFOB oscillators. This is because unlike the FFOB design, this chip has each cross-coupled transistor in the oscillator sized differently from oscillator to oscillator to ensure a uniform output without saturation clipping.

Finally, Table 4.2 below provides a complete summary of all thirty two simulated output frequencies and the component values utilized in each oscillator's LC tank. The inductor value is not included because a single 10.1 nH inductor is used in all eight oscillator circuits. The variable capacitance shown is the nominal capacitance indicated within the Cadence design environment to indicate relative varactor sizing, but the actual capacitance will vary with applied bias voltage.

Table 4.2: Simulation Summary

oscillator name	varactor bias (V)	desired freq (GHz)	actual freq (GHz)	Fixed cap used (fF)	Var cap used (fF)
rev2osc1	1.1	1.50	1.499	632	296
	1.5	1.55	1.541		
	2.2	1.60	1.592		
	3.2	1.65	1.641		
rev2osc2	1.1	1.70	1.699	485	224
	1.5	1.75	1.745		
	2.2	1.80	1.802		
	3.2	1.85	1.856		
rev2osc3	1.1	1.90	1.898	385	175
	1.5	1.95	1.942		
	2.2	2.00	2.002		
	3.2	2.05	2.061		
rev2osc4	1.1	2.10	2.104	320	123
	1.5	2.15	2.151		
	2.2	2.20	2.21		
	3.2	2.25	2.266		
rev2osc5	1.1	2.30	2.307	266	86
	1.5	2.35	2.356		
	2.2	2.40	2.412		
	3.2	2.45	2.464		
rev2osc6	1.1	2.50	2.504	218	69
	1.5	2.55	2.552		
	2.2	2.60	2.61		
	3.2	2.65	2.664		
rev2osc7	1.1	2.70	2.704	180	54
	1.5	2.75	2.753		
	2.2	2.80	2.811		
	3.2	2.85	2.865		
rev2osc8	1.1	2.90	2.911	153	40
	1.5	2.95	2.958		
	2.2	3.00	3.01		
	3.2	3.05	3.06		

Chapter 5

CONCLUSIONS

This chapter is comprised of just two sections. The first summarizes the scope of the completed work, while the second offers thoughts on the continuation of work and future endeavors.

5.1 Conclusions and Summary of Completed Work

An IC was designed, simulated, laid out, manufactured and tested to serve as a chirp signal generator of a LADAR system. This chip, dubbed the FFOB, underwent considerable testing and analysis that highlighted a number of problems with the design. While the chip was meant to output 16 discrete frequencies from 600 MHz to 2.1 GHz, only the upper half functioned reliably in the manufactured chip. Furthermore, the design consumes 990 mW of power due to design oversights.

To address these problems, a new design was created, the so-called VCOB. The new revision featured additional functionality, including an on-chip digital control block that controls the oscillators as well as vastly improved power consumption (18mW) and frequency distortion. The VCOB is capable of reliably outputting all 32 points in its bandwidth of 1.5 to 3.05 GHz. Variable output frequencies can determined by the user controlled bias voltage inputs based on the desired LADAR application. Layout and simulation work has been completed on the VCOB design, and it is ready for manufacture.

5.2 Future Work

The most obvious path forward to continue this research would be to have the new revision of the chip manufactured and tested. This work amounts to the miniaturization of just one small circuit block needed to realize an entire functioning LADAR system. Additional work at the University of Maine had been completed on other aspects of a comprehensive LADAR system. A project that incorporates this work into a larger LADAR scheme is a viable path forward. Yet another potential avenue of academic pursuit would be to further miniaturize the design presented in this thesis and use additional chip space to incorporate more of a LADAR system, with the end goal to be have an entire comprehensive LADAR system on a single chip.

BIBLIOGRAPHY

1. Ashman, Ben, "An Investigation into Variable Chirped FM LADAR: Analysis and Implementation," Internal project report, Univ. of Maine, Orono, (2009).

2. B. L. Stann et. al., "Chirped amplitude modulation ladar for range and Doppler measurements and 3-D imaging," Proc. SPIE Laser Radar Technology and Applications XII, Vol. 6550, 655005 pp. 1-12, (2007).

3. B. L. Stann et. al., "A scannerless imaging ladar using a laser diode illuminator and FM/cw radar principles", presented at SPIE AeroSense, 6-9 April 1999; Proc SPIE Laser Radar Technology and Applications IV, Vol. 3707, (1999).

4. Zhang, Wang, "InP/In 0.53 Ga 0.47 As Symmetric Gain Optoelectronic Mixers for LADAR Applications", The University of Maine, (2010).

5. Yue, Patrick, "VCO Design Overview", University of California Santa Barbara, Electrical and Computer Engineering Lecture Series, (2010).

6. Ebrahimzadeh, Mahdi, "Design of an Ultra Low Power Low Phase Noise CMOS LC Oscillator", World Academy of Science, Engineering and Technology, (2011).

7. Yoon, Sangwoong, "LC-tank CMOS Voltage-Controlled Oscillators using High Quality Inductors Embedded in Advanced Packaging Technologies", Georgia Institute of Technology, (2004).

8. Salimath, Chetan, "Design of CMOS LC Voltage Controlled Oscillators", Visveswariah Technological University, India, (2006).

9. Kuphaldt, Tony, "Ring Counters", Lessons In Electric Circuits, Volume IV Digital, All About Circuits, (2007).

10. Shizen, et al, "Design of a Voltage-Controlled Ring Oscillator Based on MOS Capacitance," International MultiConference of Engineers and Computer Scientists, Hong Kong, (2009).

BIOGRAPHY OF THE AUTHOR

Joseph R. Grace III grew up in South Berwick, Maine, the son of Joseph Grace Jr. and Pamela Grace, and brother of Sandra Grace. He attended Marshwood High School and graduated valedictorian of the class of 2007. Joe received his Bachelor of Science in Electrical Engineering from the University of Maine with Honors in 2011, completing his undergraduate thesis focused on the design and prototyping of a wireless current sensor. In his spare time, Joe enjoys motorcycles, strategy games, competitive handgun shooting, and programming. Joe has accepted a full time position as a product engineer with Texas Instruments in South Portland, Maine. He is a candidate for the Master of Science degree in Electrical Engineering from the University of Maine in May 2013.