2002

Multiband Analog-to-Digital Conversion

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MULTIBAND ANALOG-TO-DIGITAL CONVERSION

By

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B.S. University of Maine, 2000

A THESIS

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

(in Electrical Engineering)

The Graduate School

The University of Maine

December, 2002

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Thesis Advisor: Dr. Donald M. Hummels

An Abstract of the Thesis Presented
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The current trend in the world of digital communications is the design of versatile devices that may operate using several different communication standards in order to increase the number of locations for which a particular device may be used. The signal is quantized early on in the reciever path by Analog-to-Digital Converters (ADCs), which allows the rest of the signal processing to be done by low complexity, low power digital circuits. For this reason, it is advantageous to create an architecture that can quantize different bandwidths at different frequencies to suit several different communication protocols.

This thesis outlines the design of an architecture that uses multiple ADCs in parallel to quantize several different bandwidths of a wideband signal. A multirate filter bank is then applied to approximate perfect reconstruction of the wideband signal from its subband parts. This highly flexible architecture is able to quantize signals of varying bandwidths at a wide range of frequencies by using identical hardware in every channel, which also makes for a simple design. A prototype for the quantizer used in each channel, a frequency-selective fourth-order sigma-delta ($\Sigma\Delta$) ADC, was designed and fabricated in a 0.5 μm CMOS process. This device uses a switched-capacitor technique to implement the frequency selection in the front-end of the $\Sigma\Delta$ ADC in each channel.

Running at a 5MHz sample rate, the device can select any of the first sixteen 156.25kHz wide bands for conversion. Testing results for this fabricated part are also presented.

ACKNOWLEDGMENTS

Part of this research was funded by the Roger Castle Fund. The assistance has been greatly appreciated.

I would first like to thank my parents, Mr. and Mrs. Gaelen Saucier for their support during my long academic career here at the University of Maine. I would also like to thank my brother Tony for being such a great friend these last few years. I would especially like to thank my wife Erin for her patience and encouragement throughout the entire process.

Many thanks go to my advisor Don Hummels, whose ideas and guidance were key to the development of this project. Thanks also to Fred Irons, for his help with this thesis, with other projects both at the undergraduate and graduate levels, and with fishing. Thanks to Dave Kotecki for serving on this committee and for his help during the design and layout of the prototype hardware. Thanks to Ron Bryant for undertaking the design of the hardware for this project with me. And last but not least, thanks to Kannan Sockalingam for suffering through Graduate School these last two years with me and for being a great friend.

This work is dedicated to the memory of my grandfather Gayland A. Moore Jr., one of the first engineers I ever knew.

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CHAPTER 1

INTRODUCTION

The increasing number of communications protocols and the expanding world of digital communications calls for companies to produce more versatile devices. Devices such as cellular telephones and software radios are often designed to operate using more than one method of reception to increase the number of locations in which the device may be used. At the time of this writing most cellular telephones can receive both analog and digital signals. Implementing a number of different receiver types in one device can be very expensive. There is definite need for easily implemented designs that accomodate several different communication protocols in a single device.

Many newer receiver architectures call for the signal to be digitized as early as possible. The remainder of the processing is left to lower power, reliable digital circuits more cheaply realized than their analog counterparts. In order for this to happen, the analog-to-digital converter (ADC) systems that quantize the incoming signals must become versatile and easy to implement.

Sigma-delta ($\Sigma\Delta$) ADCs provide a high degree of resolution using low complexity components at a high sampling rate. The biggest drawback to using these quantizers is that the increased resolution is achieved in a very narrow band of frequencies compared to the sample rate. However, the insensitivity to circuit matching makes this converter a good candidate for multiband conversion. The outputs from multiple quantizers run in parallel can be combined to achieve the high resolution of the $\Sigma\Delta$ ADC over a much wider bandwidth.

This thesis investigates an architecture that allows the use of a bank of $\Sigma\Delta$ ADCs to quantize several narrow bands of frequencies. Digital filtering and sample rate conversion are then applied to approximate the perfect reconstruction of adjacent quantized bands to reproduce the wideband signal in the digital domain. Using this

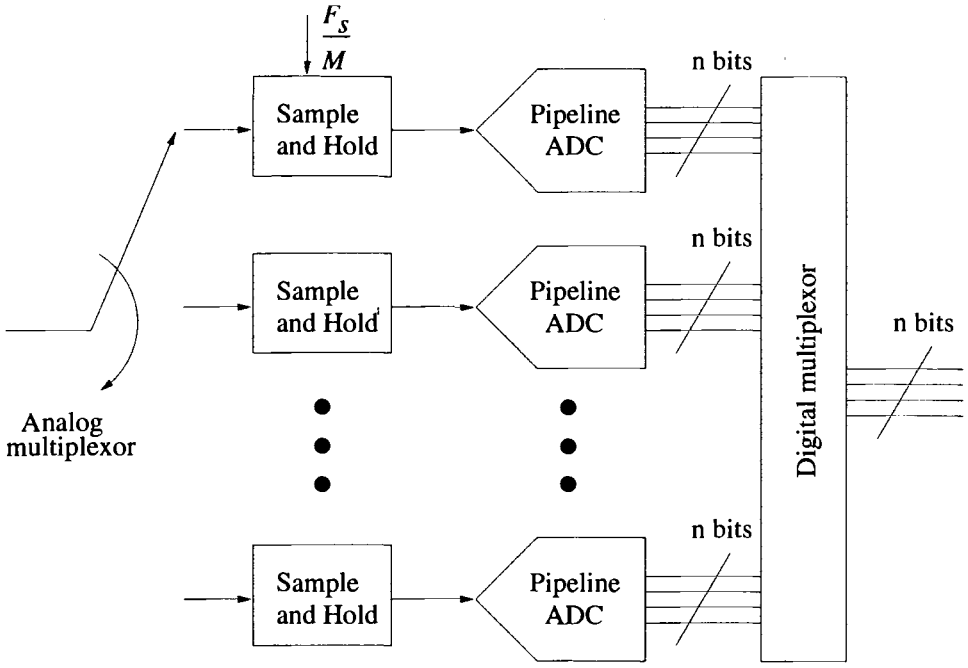


Figure 1.1: Time-interleaved parallel pipeline ADC structure

architecture, a number of different frequency bands with different widths, centered at different frequencies, may be received, digitized, and subsequently processed, all by the same device. This kind of versatility can be exploited to suit several different communication protocols, with the different receiver types implemented in software all using the same hardware.

1.1 Background

The goal of this thesis is to implement a sampling architecture that achieves sample rates that are higher than technology allows for a single device. This can be accomplished by using multiple ADCs in parallel and interleaving their measurements in the time domain or using analysis techniques on individual bands in the frequency domain.

1.1.1 Time-interleaved structure

Time-interleaved ADCs use multiple quantizers sampling at alternating intervals to increase sampling rates. Figure 1.1 shows the time-interleaved structure of parallel pipeline converters by Lin [2]. Pipeline ADCs were used because they offer high speed (greater than 10 MHz) and high resolution (10 bits or greater). Each channel samples at a rate $\frac{F_s}{M}$, where F_s is the sample rate of the entire structure and M is the number of channels. The sampling instant of each sample and hold block is shifted in time such that each converter takes a sequential sample in time. The outputs from each channel are collected and sequenced in digital hardware to give quantized output at a rate that is M times that of a single device.

In order for the time-interleaved structure to provide high resolution, matching between devices is of great concern. Work in [2] shows that pipeline ADCs are best suited for use in the time-interleaved structure, as they provide a high sample rate with an efficient use of chip area for a given technology. The converters used in this architecture must be wideband devices for this structure to achieve higher sampling rates. The $\Sigma\Delta$ is therefore not a good choice for the time-interleaved structure.

1.1.2 Frequency analysis structure

An alternative to the time-interleaved structure is one that uses a bank of ADCs in parallel to operate on separate frequency bands in what is referred to as a frequency analysis structure. The range of input frequencies is broken into a set of subband signals for analysis. A block diagram of the basic structure appears in Figure 1.2. All the ADCs in the structure are identical devices that operate on different subband signals. The filters $H_k(z)$ are the analog decomposition filters, and the filters $G_k(z)$ are the digital recombination filters. Because there is no modulation of signals to lower frequencies, the need for high-speed, high-precision sample-and-hold circuitry still exists [3]. Researchers

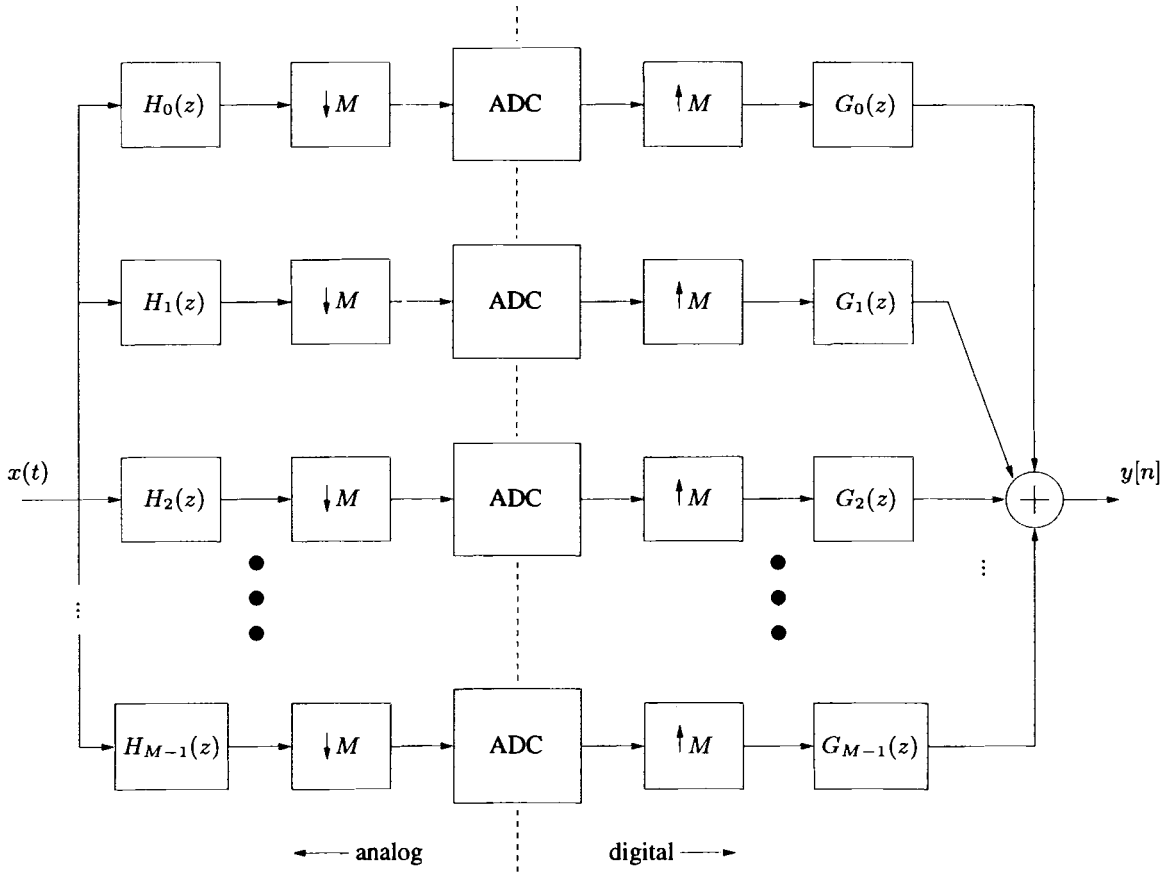


Figure 1.2: M-channel frequency analysis ADC structure

have argued that using identical quantizers in each channel offers a more flexible architecture.

1.1.3 $\Sigma\Delta$ ADCs used for channel quantizers

$\Sigma\Delta$ ADCs are able to quantize signals with a high degree of resolution, provided the signal energy is located at low frequencies compared to the sample rate. Using an integrating feedback loop, this converter applies a delay to the signal input and a noise shaping transfer function to the quantization noise. Signals that reside outside the narrow baseband region that is quantized with high resolution are pushed into the quantization noise that is shaped away from baseband. Using a one-bit quantizer and a one-bit digital-to-analog converter (DAC), $\Sigma\Delta$ ADCs are capable of achieving greater than 16-bits of resolution [4].

The $\Sigma\Delta$ ADC has been previously employed in a multiband scheme that used one lowpass converter and several bandpass devices [5]. A high degree of resolution was achieved across a bandwidth quantized by four devices. This work supports the idea that the $\Sigma\Delta$ ADC is a strong candidate for the quantizer used in each channel of the proposed structure due to the high resolution achieved by the converter. It is well suited to Very Large Scale Integration (VLSI) technology as it uses circuits that do not have to be well matched to produce high precision outputs.

1.2 Purpose of the research

The purpose of this research is to formulate an architecture that makes use of identical quantizers operating in parallel to efficiently perform wideband conversion. Each channel in the architecture contains identical hardware, so the cost of additional bandwidth is additional channels. The desired result is a structure that is able to recombine a number of smaller bandwidth signals into one with larger bandwidth. The recombined signal should have as little magnitude and phase distortion as possible across the total

recombined bandwidth, including where the edges of the smaller bands meet. The main focus of this thesis is the digital processing that allows the resolution of these parallel devices to be reliably extended to cover the first Nyquist band, which is half of the sample rate.

1.3 Thesis organization

Chapter 2 looks at bandpass signals and the quantization of those signals. The complex representation of bandpass signals is explained as well as the notation used throughout the remaining chapters to denote these signals. Different methods of sampling bandpass signals are discussed. Chapter 3 discusses the use of digital filter banks and their design. Multirate systems are discussed and an overview of the design of the proposed stucture is given. Chapter 4 gives an example of a filter bank designed specifically for the $\Sigma\Delta$ modulator designed for this project [1]. The performance of the recombination filter bank is examined. In support of this work, a monolithic frequency selective IQ $\Sigma\Delta$ modulator was designed and fabricated in a 0.5 μm CMOS process from AMI Semiconductor. This device is the prototype for the lowpass $\Sigma\Delta$ ADC unit used to quantize each band that is recombined digitally. Chapter 5 briefly examines the IC fabricated specifically for the architecture described in this thesis. The methods and results of the testing of the fabricated device are explained. Chapter 6 draws conclusions about the work presented in this thesis, and proposes ideas for future work.

CHAPTER 2

BANDPASS SIGNALS

This chapter provides an overview of bandpass signal quantization. The complex representation of bandpass signals is discussed in order to develop notation for later chapters and to provide insight on how bandpass signals are quantized. Different methods of sampling bandpass signals are discussed, and finally an outline of the proposed wideband ADC architecture is given.

2.1 Complex representation of bandpass signals

A frequency spectrum $X_c(F)$ of a real, continuous time bandpass signal, $x_c(t)$, is illustrated in Figure 2.1. A real signal with energy centered at frequency F_o also has energy at the conjugate frequency, $-F_o$. According to the Nyquist sampling theorem, a signal must be sampled at a rate that is at least twice the maximum frequency of the signal in order to quantize the signal without losing any information [6]. For a signal centered at frequency F_o with bandwidth B, the sample rate must be

$$F_s \geq 2\left(F_o + \frac{B}{2}\right), \tag{2.1}$$

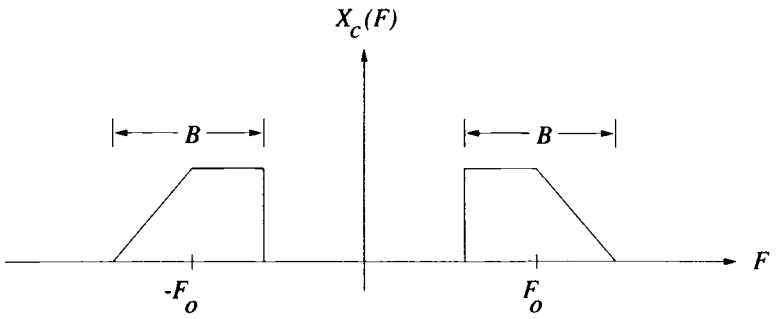


Figure 2.1: Frequency spectrum of a real bandpass signal

which may be difficult to acheive for large F_o or B. All of the information needed to accurately represent $x_c(t)$ is contained in the positive frequencies centered at F_o, while the information contained in the negative frequencies centered at $-F_o$ is a conjugate copy of that information. Since there is no need to retain both halves of the signal spectrum, one half of the energy shown (centered at either F_o or $-F_o$) is enough to represent the signal, and the remaining half is redundant and can be ignored. Translation of the spectrum to the origin and lowpass filtering allows $x_c(t)$ to be represented at a much lower sampling rate. The highest frequency of interest is now $\frac{B}{2}$, and the sampling rate must be at least twice this amount or

$$F_s \geq 2\left(\frac{B}{2}\right) = B. \tag{2.2}$$

This rate is usually considerably lower than the previous sampling rate and allows for more efficient processing of the signal. The corresponding lowpass signal, denoted $\tilde{x_c}(t)$, is given by

$$\tilde{x}_c(t) = L.P.P.\{x_c(t)e^{-j2\pi F_o t}\} \tag{2.3}$$

where $\tilde{x}_c(t)$ is the "lowpass part" of the translated signal. The signal $\tilde{x}_c(t)$ is complex valued and is generated by lowpass filtering a complex modulated signal.

2.1.1 Complex modulation

Translation of the frequency spectrum in the manner described above is acheived by complex modulation (also known as vector modulation). Euler's identity below gives the relations that are used to generate the translated signal.

$$\begin{aligned} \cos(\theta) &= \frac{e^{j\theta} + e^{-j\theta}}{2} \\ \sin(\theta) &= \frac{e^{j\theta} - e^{-j\theta}}{2j} \end{aligned} \tag{2.4}$$

Combining the cosine and sine waves allows separation of the complex exponential terms in (2.4). This separates the signal into its in-phase and quadrature parts, so named because the two terms have a 90 degree phase difference and thus are in quadrature with respect to each other. Either exponential term can be extracted using a combination of cosine and sine wave signals:

$$\begin{aligned} \cos(2\pi F_c t) + j\sin(2\pi F_c t) &= e^{j2\pi F_c t} \\ \cos(2\pi F_c t) - j\sin(2\pi f_c t) &= e^{-j2\pi F_c t}. \end{aligned} \tag{2.5}$$

Modulation of $x_c(t)$ with either of the complex sums shown in (2.5) yields a shift of the entire spectrum of $x_c(t)$ in just one direction because only one of the complex exponential terms are present in the modulation. This method eliminates the possibility of aliasing terms onto each other and allows the bandpass signal centered at F_o to be mixed all the way down to the origin. The concept of complex modulation using the separated exponentials is illustrated in Figure 2.2. The frequency spectrum $X_c(F)$ appears in Figure 2.2a. The complex exponential that modulates $x_c(t)$ has energy only at the frequency $-F_c$ and none at the conjugate frequency F_c as shown in Figure 2.2b. When the two spectrums are convolved, as shown in Figure 2.2c, the resulting signal is complex valued in the time domain since the resulting spectrum is no longer symmetrical about the origin. The spectrum $X_c(F)$ has been shifted in only one direction, towards $F = -\infty$, using the second complex sum from (2.5). (Note that using the first complex sum would simply result in the output spectrum shifted in the opposite direction, towards $F = +\infty$.)

The lowpass signal $\tilde{x}_c(t)$ is generated from a translated version of the sequence $x_c(t)$ using complex modulation by allowing $F_c = F_o$. As a result $\tilde{x}_c(t)$ is usually complex-valued when $x_c(t)$ is real. After the translation $\tilde{x}_c(t)$ is created by lowpass

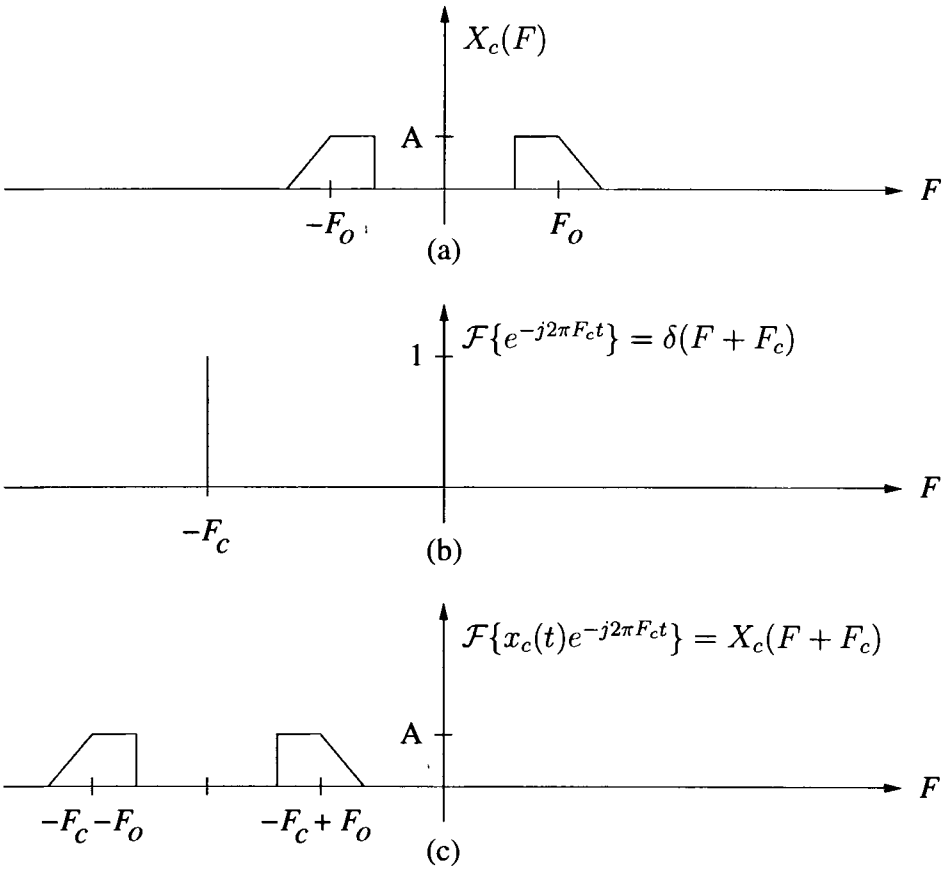


Figure 2.2: Complex IQ modulation

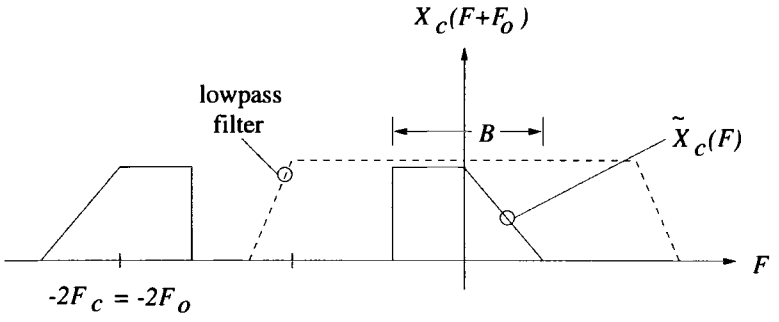


Figure 2.3: Lowpass representation of $X_c(f)$

filtering the portion of $X_c(F)$ that now resides at the origin with bandwidth B as shown in Figure 2.3.

2.1.2 Properties of bandpass representations

It can be shown that the original sequence, $x_c(t)$, can be recovered by translating $\tilde{x}_c(t)$ back to F_o and taking the real part of that complex-valued signal

$$x_c(t) = 2Re\{\tilde{x}_c(t)e^{j2\pi F_c t}\}. \tag{2.6}$$

The signal given in (2.6) can be interpreted as

$$x_c(t) = 2|\tilde{x}_c(t)|\cos(2\pi F_c t + \angle\tilde{x}_c(t)) \tag{2.7}$$

where $2|\tilde{x}_c(t)|$ is the envelope of the bandpass representation of $x_c(t)$ and $\angle\tilde{x}_c(t)$ is its phase.

The reduced bandwidth of the complex representation makes it attractive for quantizers that sample bandpass signals to produce samples of $\tilde{x}_c(t)$ rather than $x_c(t)$. The sampled version of $\tilde{x}_c(t)$ is found by evaluating the signal at discrete points in time

$$\begin{aligned} \tilde{x}[n] &= \tilde{x}_c(nT_s) \\ &= L.P.P.\{x_c(nT_s)e^{-j2\pi f_o n}\} \end{aligned} \tag{2.8}$$

where

$$\begin{aligned} T_s &= \frac{1}{F_s} \\ f_o &= \frac{F_o}{F_s}. \end{aligned} \tag{2.9}$$

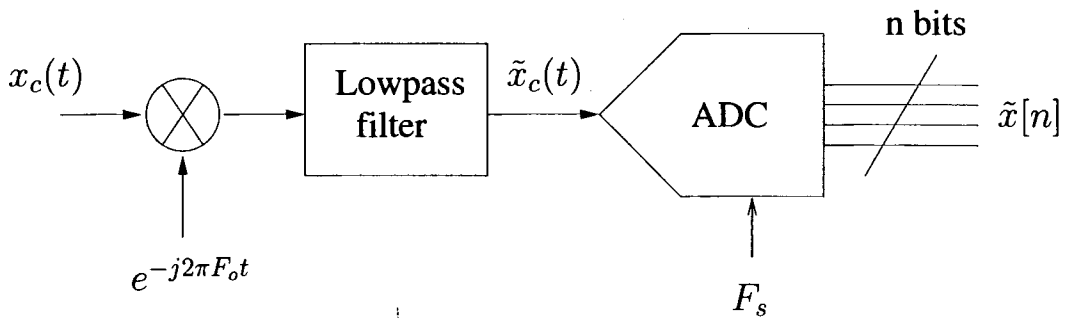


Figure 2.4: Sampling of bandpass signals

The structure shown in Figure 2.4 illustrates a bandpass sampling system as described above. The mixer and lowpass filter generate the signal $\tilde{x}_c(t)$ and the quantizer samples the lowpass signal to produce $\tilde{x}[n]$. Unfortunately $\tilde{x}[n]$ cannot be created in this manner because ADCs cannot distiguish between real and complex waveforms and are incapable of sampling complex signals by themselves. The following section discusses methods used to sample a bandpass signal using the complex respresentation of that signal.

2.2 Bandpass sampling schemes

Sampling bandpass signals requires a different approach than lowpass signals due to the frequency of the bandpass signal. Signals at frequencies much higher than the sampling rate of the converter may need to be sampled, which can be complicated. Several techniques for sampling high frequency bandpass signals are now discussed.

2.2.1 IQ ADC structure

A fairly common bandpass sampling structure is given in Figure 2.5. It consists of an "in-phase" channel and a "quadrature" channel each feeding an ADC. The modulation by cosine and sine waves generates the terms for the complex modulation that shifts the spectrum down to the origin as explained in Section 2.1.1. The in-phase channel

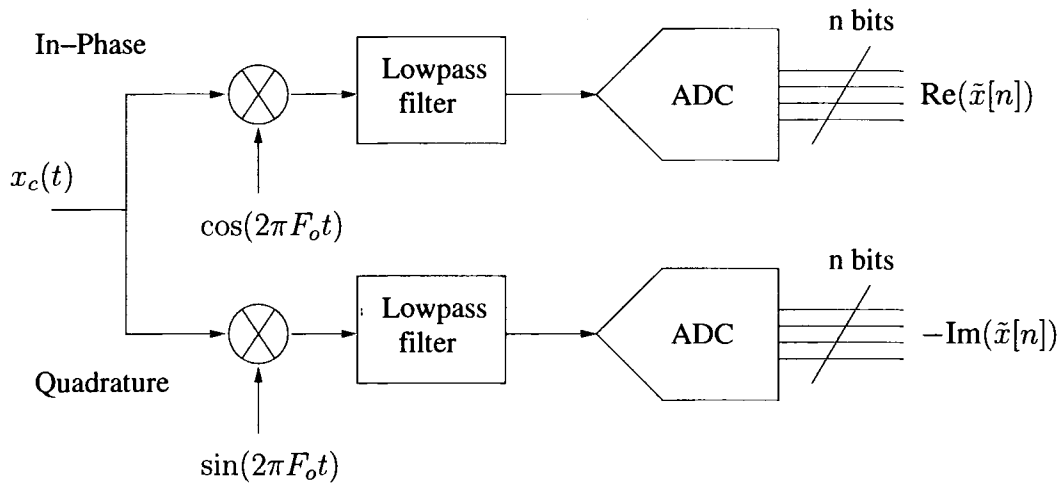


Figure 2.5: Bandpass ADC IQ Structure

contains all the real bits of the output, while the quadrature channel contains all the imaginary bits. The complex signal can be obtained by adding the real portion with a phase-shifted version of the imaginary portion.

$$\tilde{x}[n] = \text{Re}(\tilde{x}[n]) + j\text{Im}(\tilde{x}[n]) \tag{2.10}$$

Matching between the in-phase and quadrature channels is of great importance, as deviation from 90 degrees in the difference between the two channels can result in unwanted image frequencies. Gain mismatch between the two local oscillators can cause large tones at DC and $\frac{f_s}{2}$ that may couple with the input signal and induce unwanted image frequencies. Analysis of both problems has been previously investigated [7]. These problems can arise as the result of analog circuitry imperfections in implementations of the in-phase and quadrature mixers.

2.2.2 Subsampling IQ structure

One solution to reduce the sensitivity of demodulation to analog modulators in the IQ structure is to perform the multiplication in the digital domain after sampling.

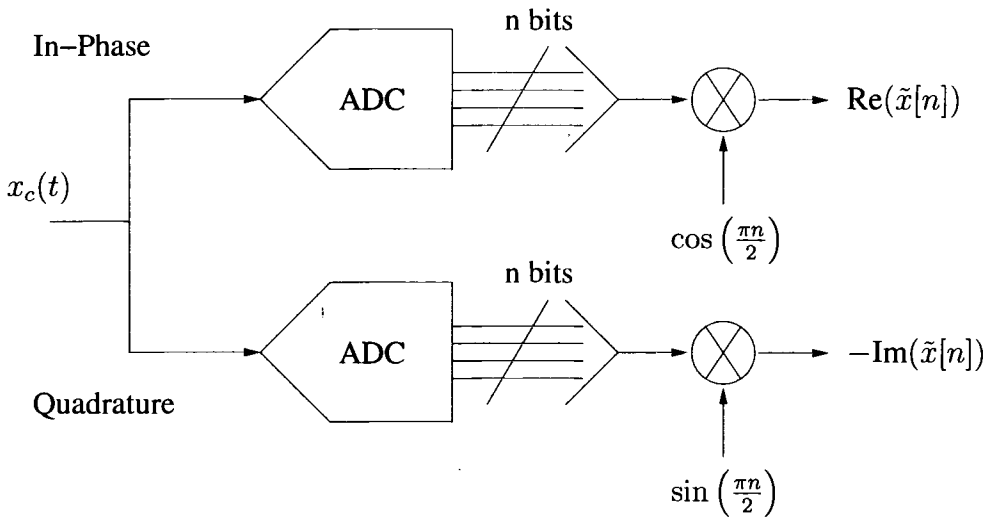


Figure 2.6: $\frac{F_s}{4}$ subsampling ADC IQ structure

This presents a problem when sampling high frequency signals, as the data rate must be increased accordingly. This technique, illustrated in Figure 2.6, makes use of subsampling in order to represent the bandpass signal at a lower frequency. When an analog signal is sampled, it is in effect multiplied by a sequence of delta functions, which causes the frequency spectrum of the sampled signal to be repeated at a period equal to the sample rate, F_s. A signal with energy at a frequency that is an integer multiple of F_s will therefore show energy at DC when sampled. By subsampling the bandpass signal, it can be quantized by a converter operating at a data rate much slower than the maximum frequency of interest in the signal. The technique of subsampling is used to perform most of the frequency translation on the bandpass signal, as mixing it all the way down to baseband would cause aliasing of the signal.

Once the signal has been quantized, complex modulation is used to mix the signal down to DC as in the IQ structure. As described below, a popular choice is to select the sample rate so that the bandpass signal is aliased onto a bandwidth centered at $\frac{F_s}{4}$. At this point complex modulation is performed in the digital domain, which can be done more reliably than with analog multipliers. The signal needs to be translated by $\frac{F_s}{4}$ which corresponds to multiplying the sequence by the complex exponential $e^{-j2\pi(\frac{1}{4})n}$

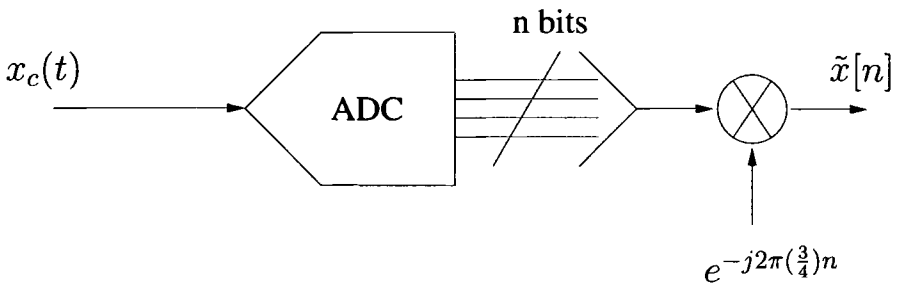


Figure 2.7: $\frac{3F_s}{4}$ subsampling ADC IQ structure

which can be accomplished by using cosine and sine modulation in each channel:

$$\cos\left(\frac{\pi}{2}n\right) - j\sin\left(\frac{\pi}{2}n\right) = e^{-j\frac{\pi}{2}n}. \tag{2.11}$$

The frequency $\frac{F_s}{4}$ is chosen because the modulating signals are easily generated. The signals are simply a stream of three values as shown below.

$$\begin{aligned}\cos\left(\frac{\pi}{2}n\right) &= 1, 0, -1, 0, 1, 0, -1, 0, \ldots \\ \sin\left(\frac{\pi}{2}n\right) &= 0, 1, 0, -1, 0, 1, 0, -1, \ldots\end{aligned} \tag{2.12}$$

The use of ones and zeros eliminates the need to store any filter coefficients in memory.

Due to the non-overlapping nature of the cosine and sine wave streams in (2.12), they can be combined into one digital stream consisting of

$$e^{-j2\pi(\frac{3}{4})n} = 1, j, -1, -j, 1, j, -1, -j, \ldots \tag{2.13}$$

By sampling the bandpass signal so that it is centered at $\frac{3F_s}{4}$, only one channel is needed because the complex modulation is performed digitally. One quantizer can produce the samples at a reduced rate using half as much hardware as needed for the $\frac{F_s}{4}$ subsampling architecture. The simplified structure appears in Figure 2.7.

At this point there are a few issues that should be considered using this toplogy in a multimode receiver. The input of the structure requires filtering to insure that nothing in any of the lower bands aliases into the signal during sampling. This filter is normally bandpass and attenuates everything but the desired signal band, which may be difficult at higher frequencies. For converting many bands, each ADC must operate at a different data rate, meaning the converters may not be the same in each channel.

2.2.3 $\Sigma\Delta$ bandpass sampling

Bandpass versions of the $\Sigma\Delta$ converter have been developed that can quantize a bandpass signal with high resolution, as it shapes quantization noise away from a particular center frequency. These converters acheive a bandwidth of high resolution that is limited to a small fraction of the sample rate, similar to that of the lowpass converter [8].

$\Sigma\Delta$ converters use low complexity circuits easily realized in VLSI technology to quantize signals with a high degree of resolution. They operate by sampling a signal at a rate that is many times higher than the bandwidth of the signal, which makes it an oversampled converter. An integrating feedback loop is used to average the samples taken by a one-bit quantizer to provide appropriate noise shaping in order to obtain a high resolution output. The oversampling spreads quantization error over a larger range of frequencies than critically sampled converters, and the integration and feedback push noise away from DC in what is called "noise shaping." By altering the loop transfer function of a lowpass $\Sigma\Delta$ converter, a quantizer that provides noise shaping at a frequency other than DC can be constructed. These bandpass $\Sigma\Delta$ converters provide high resolution for a band of frequencies that is much smaller than the data rate.

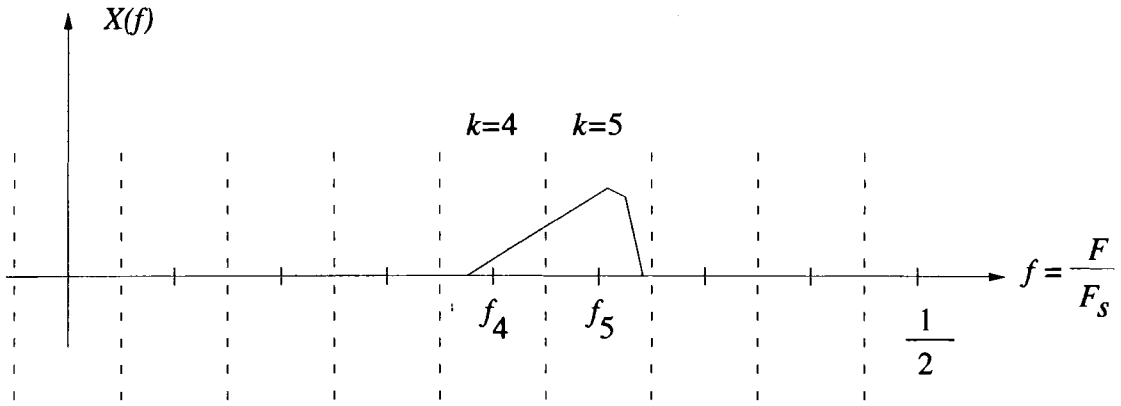


Figure 2.8: Spectrum division for subband quantization

2.2.4 ΣΔ IQ structure

The particular architecture implemented in this thesis uses ΣΔ ADCs in an IQ structure. Different parts of the signal are modulated down to baseband where they are quantized by the ADCs in the in-phase and quadrature channels. The output of the structure is the complex representation of a bandpass signal quantized with the resolution of the ΣΔ converter. This structure can only quantize narrow bandwidth signals, much like the bandpass ΣΔ. The frequency band that this structure operates on is variable, unlike the bandpass unit which operates on a fixed center frequency. Work done in [1] shows that the mixers in Figure 2.5 can be implemented in the front-end of a switched-capacitor ΣΔ ADC as will be explained in Chapter 5.

2.3 Proposed structure

In order to quantize a signal with wide bandwidth, it is necessary to use multiple ADCs running in parallel to quantize the signal. This system follows the frequency analysis approach to wideband quantization by dividing the input frequency range into a number of bands. The spectrum can be divided into M bands, each with bandwidth

equal to $\frac{F_s}{M}$. The band centers are given by

$$F_k = \frac{F_s k}{M} \qquad k = 0, 1, 2, ... \frac{M}{2} - 1 \tag{2.14}$$

where only the first $\frac{M}{2}$ bands are converted due to the fact that the second Nyquist band contains redundant information once the signal has been sampled. The division of the frequency spectrum is illustrated in Figure 2.8, where the spectrum of the quantized signal, $x[n]$, has energy located in two different bands. Each band is processed by a separate channel containing the bandpass sampling modules. In each sampling module, the signal is demodulated in order to allow the quantizer in that channel to operate on a lowpass signal. The same type of converter can therefore be used to quantize different parts of the signal while operating at the same sample rate.

The $\Sigma\Delta$ IQ ADC structure is employed to sample each bandpass section of the full signal. This method requires two ADC devices per channel for creating the in-phase and quadrature samples. The channels should be divided such that each channel is no larger than the bandwidth of the lowpass $\Sigma\Delta$ ADC which, due to the noise shaping, is normally considered to be

$$B_{\Sigma\Delta} = \frac{1}{2\text{OSR}} \tag{2.15}$$

where OSR is the over-sampling rate of the converter. The obvious choice for the channel width is to set the number of channels, M, equal to the over-sampling rate, meaning that the ADC conversion bandwidth and the channel bandwidth are the same.

The filtering in each channel provides a means for selecting each bandpass part of the signal that will be recombined. It also serves to prevent aliasing of the signal when the signal is decimated. The most important consideration in the design of the filter banks is that the pieces of the original signal are recombined without causing any distortion at the edges of the bands. Adjacent signal bands must be filtered such that the edges add to reconstruct the information properly.

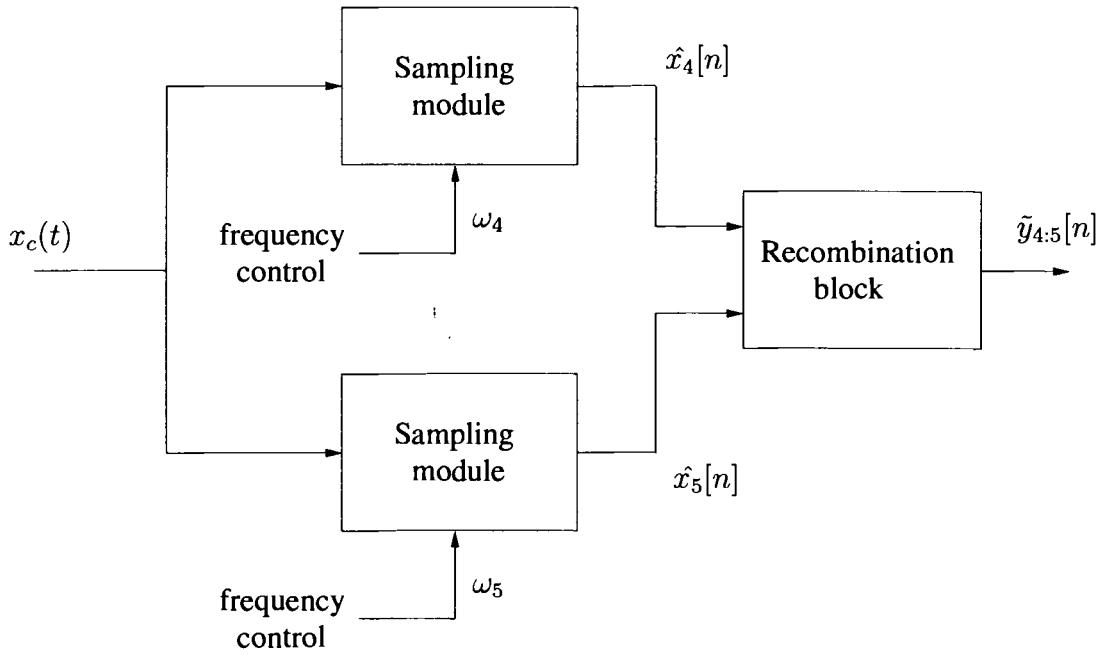


Figure 2.9: Recombination of 2 bands with proposed architecture

Figure 2.9 shows two channels of the M-channel structure. The signals $\hat{x}_4[n]$ and $\hat{x}_5[n]$ are decimated versions of the complex subband signals $\tilde{x}_4[n]$ and $\tilde{x}_5[n]$, respectively. The sampling module operates on a particular bandwidth of the signal centered at ω_k in order to produce samples of $\tilde{x}_k[n]$. The sampling module translates the signal band to baseband before quantization, and then decimates it in preparation for the recombination block. The signal $\tilde{y}_{k:k+1}[n]$ is the recombined output of channels k through $k+1$, where the subscript $k:k+1$ is used to denote the channels that the recombined output spans. The signal $\tilde{y}_{4:5}[n]$ can then be recombined with the signal $\tilde{y}_{6:7}[n]$ from the adjacent recombination block in order to create the signal $\tilde{y}_{4:7}[n]$ as shown in Figure 2.10. These blocks are simply cascaded in a tree structure to recombine additional bands.

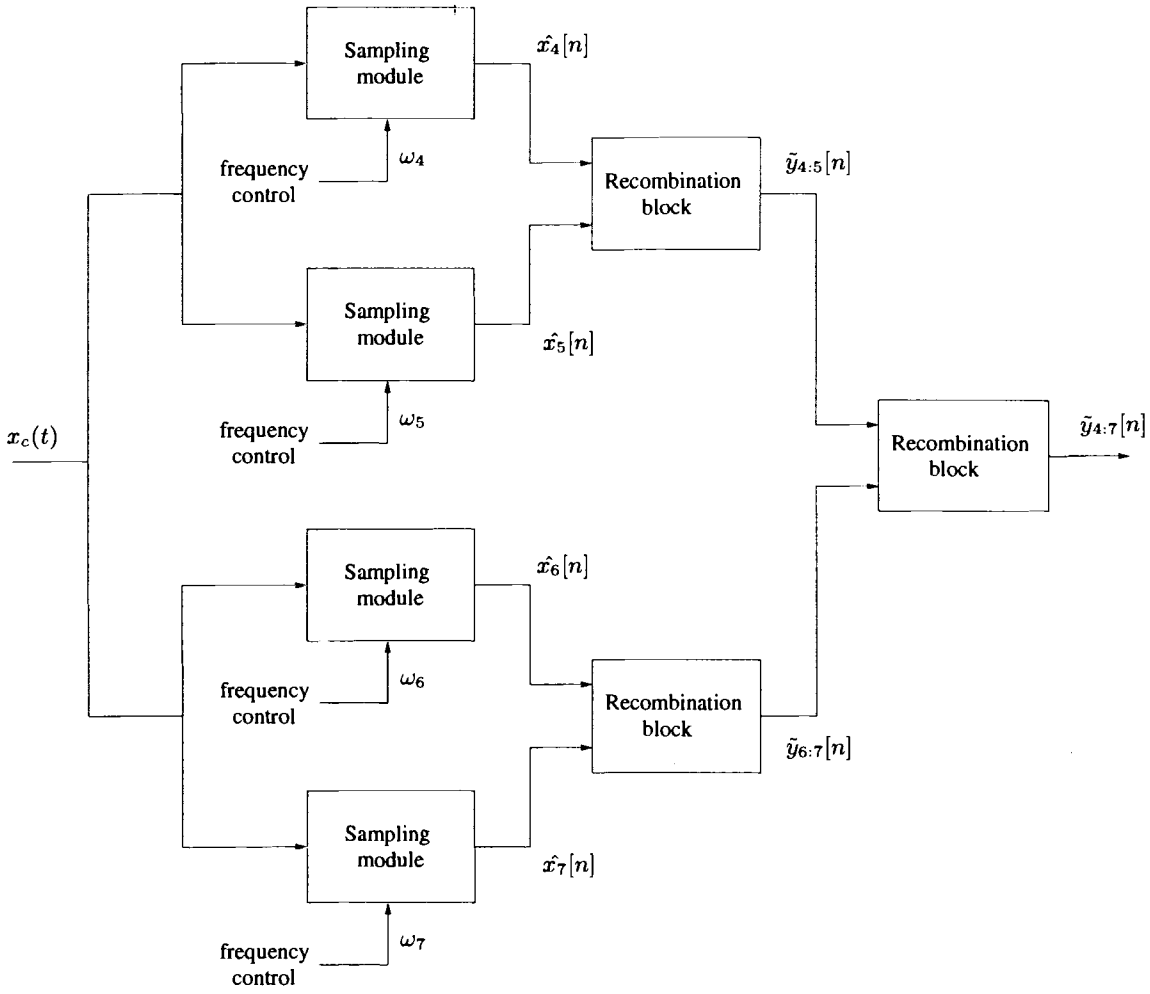


Figure 2.10: Recombination of 4 bands with proposed architecture

CHAPTER 3

FILTERING

This chapter discusses digital filter banks and their applications in digital signal processing. A few different architectures are discussed, and important design aspects for a filter bank that performs the recombination for this application are given.

3.1 Digital filter banks

Filter banks are important tools in digital signal processing that allow signals to be separated into their smaller parts for simpler processing, often at a reduced data rate. A digital filter bank normally consists of a set of bandpass filters processing a common input signal or feeding a summed output. The bandpass filters usually pass non-overlapping signal bands.

Filter banks are primarily broken into two catagories, which are analysis filter banks and synthesis filter banks. An analysis filter bank, shown in Figure 3.1a, takes one signal and filters it into several smaller bandwidth signals. Figure 3.1b shows a synthesis filter bank which performs the opposite function of combining a set of subband signals into one. Usually the emphasis in the design of a filter bank is on the quality of the separation or recombination. A system which does not distort the magnitude of the signal is said to be "magnitude preserving." Such a system may scale the amplitude of the input signal. Most systems apply a sample delay to the input signal, as a finite amount of time is required to process the signal. A system that does not produce phase distortion or add a linear term to the phase of the signal is called "phase preserving." A system that preserves both the magnitude and phase characteristics of the input signal is said to "perfectly reconstruct" the input signal. A perfect reconstruction system has a transfer function that resembles

$$H(z) = az^{-d} \tag{3.1}$$

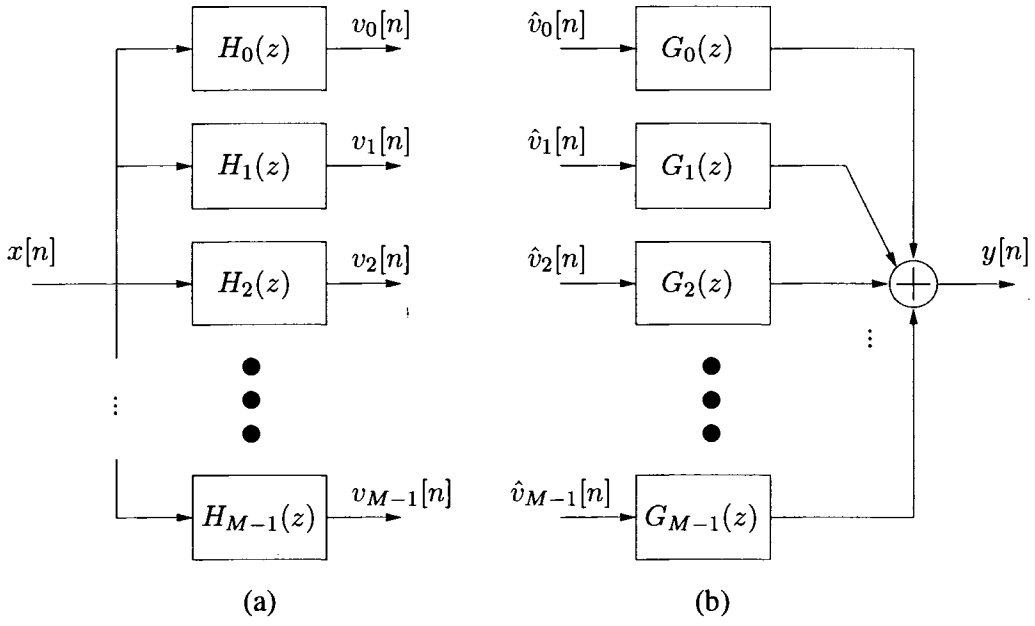


Figure 3.1: (a) Analysis and (b) synthesis digital filter banks

where a is an amplitude scaling factor and d is an integer sample delay. The output of such a system is a scaled, delayed version of the input.

3.1.1 Uniform DFT filter banks

Uniform DFT filter banks are constructed from a single lowpass prototype filter with real coefficients. The frequency response of the prototype filter is then translated in frequency to M uniformly spaced points across the frequency spectrum from DC ($k = 0$) to just below f_s ($k = M - 1$). This is accomplished through complex modulation using the exponential

$$e^{-j\frac{2\pi}{M}kn} = W_M^{kn} \tag{3.2}$$

where the commonly used notation

$$W_\lambda = e^{-j\frac{2\pi}{\lambda}} \tag{3.3}$$

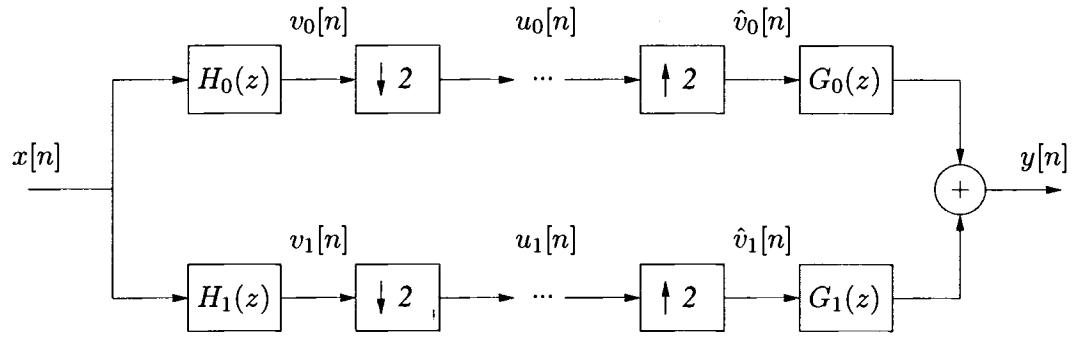


Figure 3.2: 2 channel QMF bank

has been used. The resulting filters (other than $k = 0$) all have complex coefficients and equal passband widths of $\frac{F_s}{M}$. The input signal is then processed by these filters in parallel which disects the signal into M bands for analysis. These filters are easily designed and implemented, since only one filter must be designed. This filter is a lowpass filter with bandwidth $\frac{F_s}{2M}$.

In a variation of the uniform DFT filter bank, the same lowpass prototype filter is again designed. Instead of translating the frequency characteristic of the filter to select different bands, the input signal is translated so that the band of interest for each channel falls in the passband of the lowpass filter. The analysis filter bank consists of M copies (where M is the number of channels) of the lowpass prototype filter and the complex mixers that proceed the filters, each using a different local oscillator frequency

$$\begin{aligned} \omega_k &= \frac{2\pi F_k}{F_s} \\ &= \frac{2\pi k}{M} \qquad k = 0, 1, 2, \ldots M-1. \end{aligned} \tag{3.4}$$

The synthesis filter bank for this architecture also requires complex mixers in order to shift the pieces of the input signal back to their original postitions.

3.1.2 Quadrature mirror filter banks

A 2 channel quadrature mirror filter (QMF) bank, shown in Figure 3.2, is an example of a multirate system [6]. The signal is processed at different rates throughout the system in order to acheive more efficient processing. This family of filter banks is so named because of the frequency response of the filters that comprise them. For the most basic two-channel version, the filters are symmetric about the quadrature frequency of $\omega = \frac{\pi}{2}$. In the analysis filter bank, the input signal spectrum is divided in half, with the lower frequencies and the upper frequencies processed by separate channels. Because each channel only handles half of the input spectrum, the data can be coded at half the input sample rate. At this point the signals are either transmitted or further processed. When signals are received at the synthesis filter bank, the goal is to recombine data from the two channels to reconstruct the original signal. The sample rate is doubled in both channels before interpolation filters select portions of each channel for recombination. These filters must prepare the two halves of the spectrum to be recombined at the orignal sample rate.

The equations that guide the design of the QMF bank are easily obtained through z-transform analysis of the signals at various points in the channels [6]. For the purpose of this analysis it is assumed that the signal does not undergo any processing between the analysis and synthesis banks. The signal is first filtered into a highpass and a lowpass signal in each channel

$$V_k(z) = H_k(z)X(z) \tag{3.5}$$

where k is either 0 or 1 to designate the channel that passes DC or high frequency respectively. The signal is now divided between the two channels, with each channel processing half of the original signal. In order to achieve more efficient coding, the signals are decimated by a factor of 2. The down-sampling relation for decimation by a

factor L in the z-domain is

$$X_D(z) = \frac{1}{L}\sum_{l=0}^{L-1} X(z^{1/L}W_L^{-l}). \tag{3.6}$$

The downsampled signal in one channel is then found to be

$$\begin{aligned} U_k(z) &= \frac{1}{2}[V_k(z^{1/2}) + V_k(-z^{1/2})] \\ &= \frac{1}{2}[H_k(z^{1/2})X(z^{1/2}) + H_k(-z^{1/2})X(-z^{1/2})]. \end{aligned} \tag{3.7}$$

The downsampling introduces a certain amount of aliasing of the signals in each channel depending on the filters $H_0(z)$ and $H_1(z)$. This aliasing makes simple recombination of the signals difficult, and the filters $G_0(z)$ and $G_1(z)$ must be designed to cancel out the aliasing terms upon recombination. The upsampling relation for interpolation by a factor L is given by

$$X_U(z) = X(z^L). \tag{3.8}$$

After the sample rate is doubled in the synthesis bank, the signals are given by

$$\begin{aligned} \hat{V}_k(z) &= U_k(z^2) \\ &= \frac{1}{2}[H_k(z)X(z) + H_k(-z)X_k(-z)]. \end{aligned} \tag{3.9}$$

The recombined signal $Y(z)$ is the sum of the filtered outputs from both channels

$$\begin{aligned} Y(z) &= \hat{V}_0(z) + \hat{V}_1(z) \\ &= \frac{1}{2}[H_0(z)G_0(z) + H_1(z)G_1(z)]X(z) \\ &\quad + \frac{1}{2}[H_0(-z)G_0(z) + H_1(-z)G_1(z)]X(-z). \end{aligned} \tag{3.10}$$

The relation in (3.10) is separated into two terms

$$Y(z) = T(z)X(z) + A(z)X(-z) \tag{3.11}$$

where the first term is the desired output of the system, and the second term is unwanted distortion. The signal $X(z)$ occupies the entire bandwidth, and the addition of $X(-z)$ represents aliased information in the signal. The goal is to design the filters $H_k(z)$ and $G_k(z)$ such that

$$A(z) = 0. \tag{3.12}$$

An alias-free realization of the two-channel QMF structure can be designed by choosing

$$\begin{aligned} H_1(z) &= H_0(-z) \\ G_0(z) &= H_0(z) \\ G_1(z) &= -H_1(z) = -H_0(-z) \end{aligned} \tag{3.13}$$

which meets the requirement of (3.12). The solution is then reduced to designing the filters $H_0(z)$ and $H_1(z)$ such that

$$|H_0(z)|^2 + |H_1(z)|^2 = 1. \tag{3.14}$$

Filters $H_0(z)$ and $H_1(z)$ are said to be power complimentary when (3.14) is satisfied. Filter banks using linear phase filters, with responses as given in (3.14), are perfect reconstruction filter banks [6].

The degree to which the output of the QMF bank resembles the input determines the recombination performance. Much emphasis has been placed on the design of linear phase perfect reconstruction filter banks (LPPRFBs). Straightforward analysis is only

able to produce a trivial case for which linear phase filters can be designed to satisfy the perfect reconstruction requirements. In order to find more solutions, one of the requirements is relaxed and optimization routines can find close solutions. Usually the magnitude preserving requirement of (3.14) is relaxed and linear phase filters are used as in [9]. Filter coefficients are then iteratively adjusted to provide as little distortion at the band edges as possible.

The theory behind QMF banks has been extended beyond the two-channel case to include M-channel structures. These are well suited to the recombination of several bands of digitized signals. A similar approach to the M-channel case is taken in the design of the proposed structure.

3.2 Multirate filter bank for signal reconstruction

The filter bank structure in this design is modeled after the QMF bank structure given in Section 3.1.2. Each channel is decimated to allow more efficient processing of the signal in later stages, and the filter design is governed by the transfer function of the recombined signal. The major difference between this design and the QMF bank is that the QMF bank is almost always optimized for reassembling a predetermined number of channels (which is usually the same number of channels that were separated in the system). The degree to which the signal is reconstructed depends on the frequency responses of all of the filters in the bank. The QMF bank does not perform as well if any of the channels are left out of the recombination. The design proposed in Section 2.3 allows the user to determine the number of recombined channels based on the needs of the receiver. The only limit to the number of recombined channels is that it needs to be a multiple of two, as the system recombines two adjacent bands at every stage regardless of the size of the bands. These bands double in size at every stage, so the system has a tree-like structure.

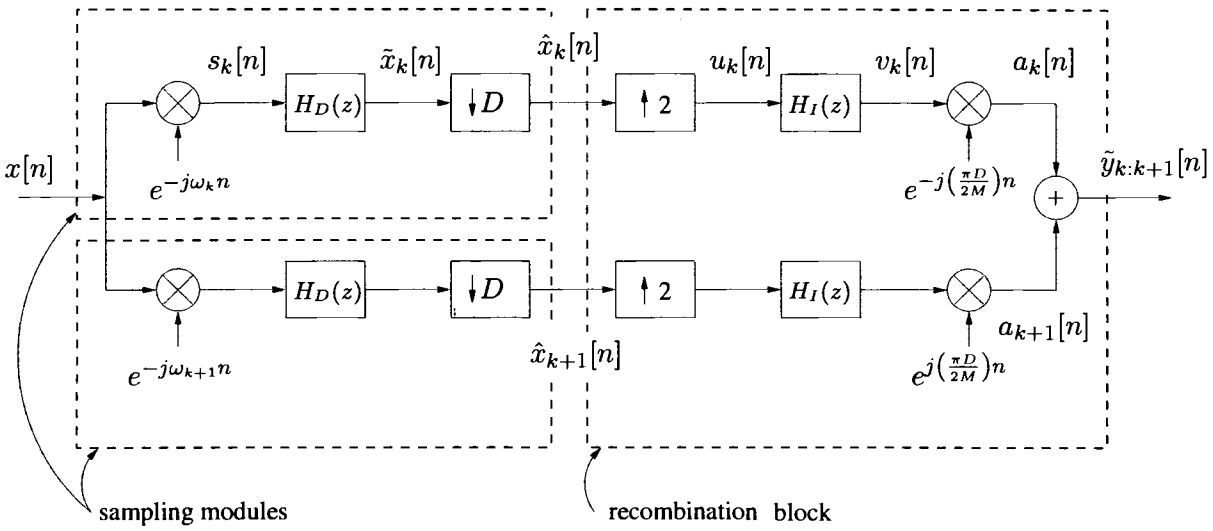


Figure 3.3: Channel recombination for a 2-channel system

The basic 2-channel structure that allows digital recombination of a wideband signal from its subband quantized parts is shown in Figure 3.3. The structure is the realization of that in Figure 2.9 used to recombine two adjacent channels. Additional channels are recombined through repeated stages of the recombination block. The demodulation and decimation at the front of the channel prepare the signal for the recombination stage. This implementation uses linear phase filters to preserve the phase information of the signal. Magnitude distortion is minimized by matching the transition edges of the filters of adjacent channels together, so the only distortion comes from passband ripple.

3.2.1 Band demodulation

The demodulation step selects the particular band that will be processed by each channel. As discussed in Section 2.1.1, complex modulation is used to obtain the lowpass complex representation of the subband signal. The entire signal is processed through in-phase and quadrature channels where it is multiplied by the complex exponential from (3.2) with the superscript k indicating which band the channel will operate on as

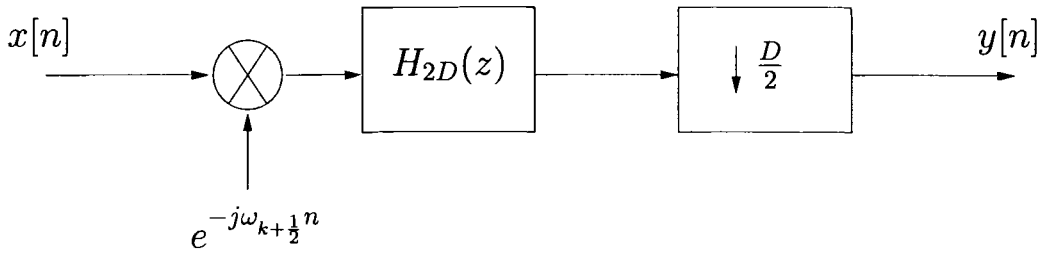


Figure 3.4: Equivalent system of Figure 3.3

in (2.14). Each channel needs two quantizers and two mixers to create the samples, although it should be noted that the two channels for in-phase and quadrature signal generation are different than the channels that recombine two adjacent parts of the signal.

The best way to implement the demodulation step is to perform the multiplication after the signal has been digitized. "Pre-sampling" the signal using a sample-and-hold (S/H) circuit, with different capacitor values, allows a digital multiplication of the signal before it reaches the quantizer. Performing the frequency translation inside the ADC may also be an option, depending on the converter topology chosen. In Figure 3.3 it is assumed that the signal has been quantized before the filter bank is applied for the purposes of the following analysis.

3.2.2 Filtering and sample rate conversion

The process of filtering the bandpass signals in the system is performed at several different sample rates. The filters $H_D(z)$ and $H_I(z)$ serve two purposes. They prevent aliasing during decimation and filter out redundant information after interpolation. They must be designed so that neighboring bands can be recombined without causing any distortion at the band edges. If the system is able to recombine two channels without distorting either subband signal, then the composite system should be equivalent to the

system of Figure 3.4, where the filter $H_{2D}(z)$ has a bandwidth that is twice that of filter $H_D(z)$.

The analysis of the two channel recombination filter bank follows very closely to that of the QMF bank. The intermediate signals along the path of each channel in Figure 3.3 are now examined. For a system consisting of M channels, the sampled bandwidth of each subband signal $\hat{x_k}[n]$ is $\frac{1}{M}$. The shifted version of $x[n]$, denoted $s_k[n]$, has z-transform

$$\begin{aligned} S_k(z) &= X(ze^{j\omega_k}) \\ &= X(zW_M^{-k}) \end{aligned} \tag{3.15}$$

where (3.4) has been substituted for ω_k. The signal $\tilde{x}_k[n]$ is the complex representation of the subband signal to be recombined, which is created by the methods discussed in Section 2.1. This signal is simply a filtered version of $s_k[n]$, where the filter $h_D[n]$ is designed to eliminate any terms that may alias onto the desired band after further processing. The decimation by a factor D allows the desired signal to fill most of the new sampling bandwidth which makes subsequent processing much easier in terms of filter coefficients and resolution. However, the down-sampling might also corrupt the signal if the filter $h_D[n]$ is not designed correctly. Decimation stretches the frequency axis but, due to the nature of the sampled signal, its frequency spectrum is always periodic with period $f = 1$. The lowpass filter $H_D(z)$ must therefore pass the signal in the range $|f| \leq \frac{1}{2M}$ and attenuate signals past the frequency $f = \frac{1}{D} - \frac{1}{2M}$. The processed bandpass signal $\hat{x_k}[n]$ appears in the z-domain as

$$\begin{aligned} \hat{X}_k(z) &= \frac{1}{D}\sum_{i=0}^{D-1} \tilde{X}_k(z^{1/D}W_D^{-i}) \\ &= \frac{1}{D}\sum_{i=0}^{D-1} H_D(z^{1/D}W_D^{-i})X(z^{1/D}W_D^{-i}W_M^{-k}). \end{aligned} \tag{3.16}$$

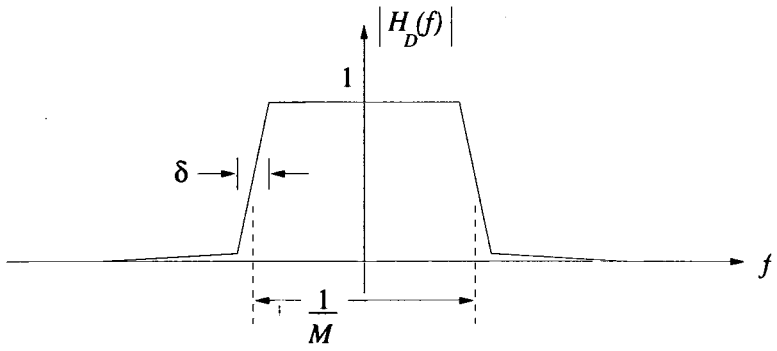


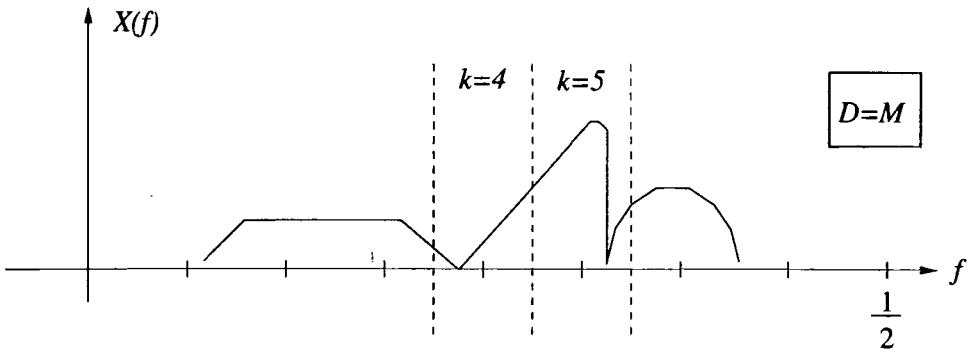
Figure 3.5: Decimation filter $H_D(z)$ frequency response

At this point it is important to note the value of the decimation rate D in relation to the number of channels M. It is allowable to have $D \leq M$, since the data in the channel will be preserved as long as the bandwidth after decimation and filtering is $\leq \frac{1}{M}$. For $D > M$ the narrow band signal will be subject to aliasing, which will distort the signal in a manner that cannot be reversed. For the following discussion on different decimation rates it is assumed that the frequency response of the filter $H_D(z)$ is as shown in Figure 3.5 where the finite transition bandwidth of the filter, denoted δ, is defined.

Case 1 - Maximally decimated filter bank

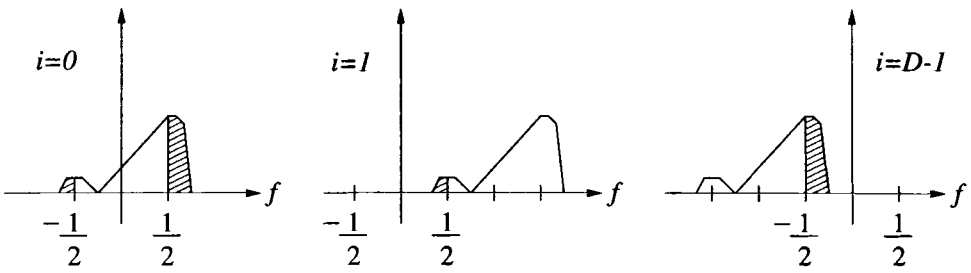
The filter bank with $D = M$ is called maximally decimated, which means that the final decimated bandwidth is as wide as each channel, with no spare room at the edges. This can be a problem when the decimation filter has a finite transition bandwidth.

The original spectrum of the sampled signal $X(f)$ appears in Figure 3.6(a), where the frequency bands of interest for $k = 4$ and $k = 5$ are noted. The adjacent signals for these particular values of k, $\hat{X}_4(z)$ and $\hat{X}_5(z)$, are targeted for recombination. Due to the filter transfer function, $H_D(z)$, only a small band of the original signal is passed to the down-sampler in each channel. The filter $H_I(z)$ also has a lowpass transfer function, so the $i = 0$ term in (3.16), which is centered at DC, is the term that the



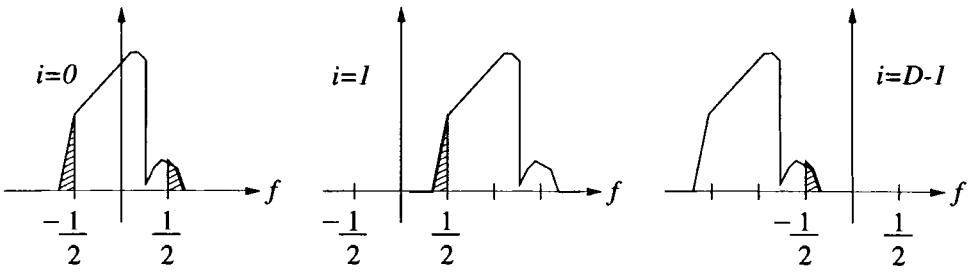
(a) Frequency spectrum of wideband signal

$$\hat{X}_4(z) = \frac{1}{D}\sum_{i=0}^{D-1} H_D(z^{1/D}W_D^{-i})X(z^{1/D}W_D^{-(4+i)})$$



(b) Potential aliasing terms of $\hat{X}_4(z)$

$$\hat{X}_5(z) = \frac{1}{D}\sum_{i=0}^{D-1} H_D(z^{1/D}W_D^{-i})X(z^{1/D}W_D^{-(5+i)})$$



(c) Potential aliasing terms of $\hat{X}_5(z)$

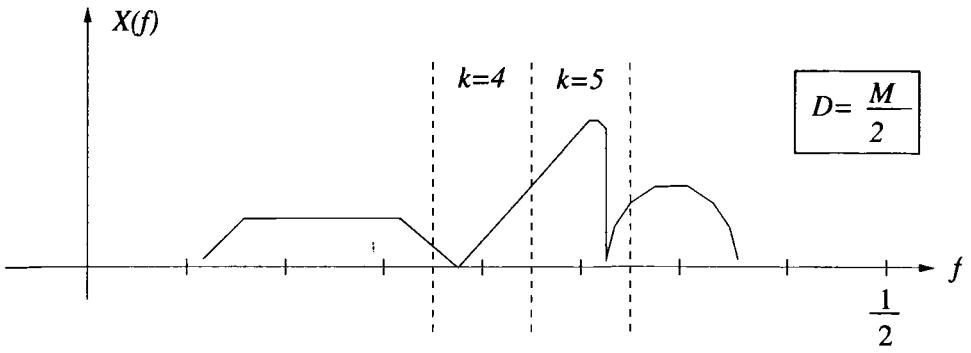
Figure 3.6: Terms of concern for aliasing using decimation with $D = M$

filter bank should preserve. When the decimated signal covers the entire first Nyquist band there may be some aliasing from the adjacent terms $i = 1$ and $i = M - 1$ in the sum. The terms of interest in the summation for $\hat{X}_4(z)$ and $\hat{X}_5(z)$ are shown in Figures 3.6(b) and 3.6(c), respectively. It can be seen that for the case where $D = M$ there is aliasing at the band edges due to these adjacent terms, where shading has been used to illustrated the areas of overlap for each term. The residue from the adjacent terms that leaks onto the $i = 0$ term is caused by the finite transition bandwidth δ of the filter $H_D(z)$. This aliasing causes distortion that cannot be undone simply by interpolation and filtering. It is for this reason that this design focuses on finding solutions for filter banks that use $D < M$.

Case 2 - Relaxed decimation

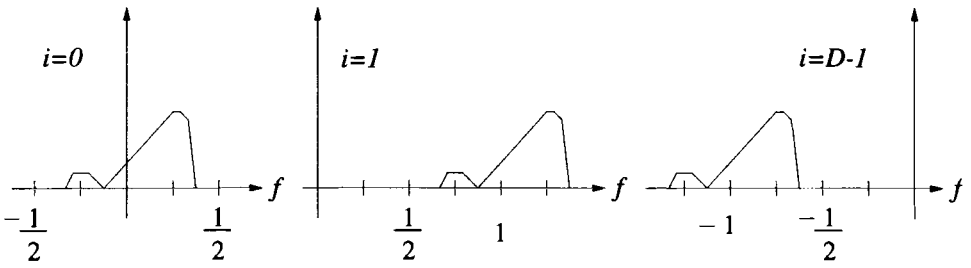
By relaxing the decimation rate compared to the number of channels, the amount of aliasing can be significantly reduced. Leaving space between each aliased term for the overlap of the transition bandwidth of the decimation filter $H_D(z)$ allows the interpolation filter $H_I(z)$ to eliminate all other terms other than desired signal. After these terms have been removed, the recombination depends on lining up the edges of signals that have been filtered by $H_D(z)$. The filter design problem then becomes finding a good design for $H_D(z)$.

Figure 3.7 illustrates relaxed decimation by $D = \frac{M}{2}$, where the same parts of the original wideband signal, shown again in Figure 3.7(a), are to be processed. The terms in Figure 3.7(b) and 3.7(c) are still centered at the same frequencies, but now they are half as wide as before. This leaves space between the three terms, and there is no overlap between terms. The stopband attenuation of filter $H_D(z)$ must be large enough so that any aliased terms will be negligable. The case for $D = \frac{M}{2}$ is the largest decimation rate that can be used without causing any aliasing of the desired term.



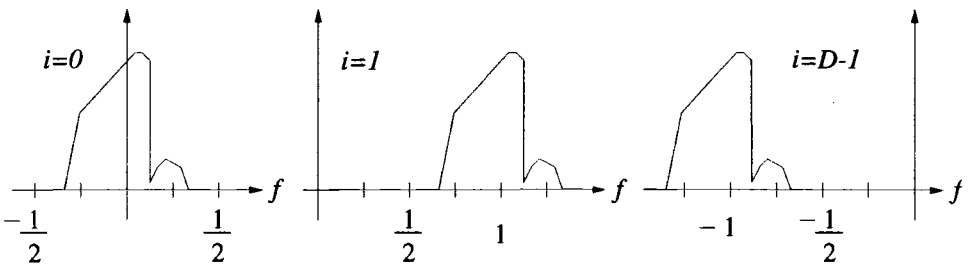
(a) Frequency spectrum of wideband signal

$$\hat{X}_4(z) = \frac{1}{D}\sum_{i=0}^{D-1} H_D(z^{1/D}W_D^{-i})X(z^{1/D}W_D^{-\left(\frac{4}{2}+i\right)})$$



(b) Potential aliasing terms of $\hat{X}_4(z)$

$$\hat{X}_5(z) = \frac{1}{D}\sum_{i=0}^{D-1} H_D(z^{1/D}W_D^{-i})X(z^{1/D}W_D^{-\left(\frac{5}{2}+i\right)})$$



(c) Potential aliasing terms of $\hat{X}_5(z)$

Figure 3.7: Terms of concern for aliasing using decimation with $D = \frac{M}{2}$

By using a decimation rate $D < M$, a linear phase filter bank can be designed that eliminates any contribution to the signal by terms other than $i = 0$ in (3.16). For the purpose of the analysis, the signal $\hat{x}_k[n]$ now appears as

$$\hat{X}_k(z) = \frac{1}{D} H_D(z^{1/D}) X(z^{1/D} W_M^{-k}) \tag{3.17}$$

provided that $D < M$. The requirements for the filter $H_D(z)$ at this point are that it needs to pass signals in the range $0 \leq f \leq \frac{1}{M} - \frac{\delta}{2}$, and that it needs to provide a large amount of attenuation to signals in the range $\frac{1}{M} + \frac{\delta}{2} \leq f \leq \frac{1}{2}$. The transition band requirements will be derived once the recombination stage has been discussed.

3.2.3 Recombination stage

The recombination stage is designed to add together two adjacent bands of the same bandwidth. As shown in Figure 3.3, the recombination begins with an interpolation step that increases the sample rate by a factor of two. This widens the sampled bandwidth to a size that is large enough to fit the signals from both channels. The signal $u_k[n]$ is an up-sampled version of the subband signal $\hat{x}_k[n]$ given in the z-domain by

$$\begin{aligned} U_k(z) &= \hat{X}_k(z^2) \\ &= \frac{1}{D} H_D(z^{2/D}) X(z^{2/D} W_M^{-k}). \end{aligned} \tag{3.18}$$

The interpolation produces another copy of the desired signal band in the sampled bandwidth, and the interpolation filter, $H_I(z)$, is included to remove that copy. The signal $v_k[n]$ is the lowpass filtered version of $u_k[n]$, meaning that $v_k[n]$ and the signal produced from the adjacent band, $v_{k+1}[n]$, each contain the lowpass versions of the subband signals for the k and $k+1$ bands. These signals are then complex modulated in different directions in order to construct the lowpass version of the signal bandwidth that

is twice as large as that in a single channel. The size of the frequency translation depends on the down-sampling rate. The two channels should be shifted by half the width of the signal band after the interpolation filter, which for the maximally decimated case, would be $f = \frac{1}{4}$. For the case of relaxed decimation, this shift is scaled by the ratio of $\frac{D}{M}$, yielding a shift of $f = \frac{D}{4M}$. The signal $a_k[n]$ in the z-domain is found to be

$$\begin{aligned} A_k(z) &= V_k(ze^{j\frac{\pi D}{2M}n}) \\ &= \frac{1}{D}H_I(ze^{j\frac{\pi D}{2M}})H_D(z^{2/D}e^{j\frac{\pi}{M}})X(z^{2/D}e^{j\frac{\pi}{M}}W_M^{-k}) \\ &= \frac{1}{D}H_I(zW_M^{-D/4})H_D(z^{2/D}W_M^{-1/2})X(z^{2/D}W_M^{-(k+\frac{1}{2})}) \end{aligned} \tag{3.19}$$

and the signal $a_{k+1}[n]$ in the opposite channel is given by

$$A_{k+1}(z) = \frac{1}{D}H_I(zW_M^{D/4})H_D(z^{2/D}W_M^{1/2})X(z^{2/D}W_M^{-(k+\frac{1}{2})}) \tag{3.20}$$

where (3.3) has been substituted into the appropriate locations. The two signals $a_k[n]$ and $a_{k+1}[n]$ are then summed, which gives the recombined two-channel output

$$\begin{aligned} \tilde{Y}_{k:k+1}(z) &= A_k(z) + A_{k+1}(z) \\ &= \frac{1}{D}[H_I(zW_M^{-D/4})H_D(z^{2/D}W_M^{-1/2}) \\ &\quad + H_I(zW_M^{D/4})H_D(z^{2/D}W_M^{1/2})]X(z^{2/D}W_M^{-(k+\frac{1}{2})}). \end{aligned} \tag{3.21}$$

The signal $X(z^{2/D})$ has twice the bandwidth of the signal in each channel, and the modulation term $W_M^{k+\frac{1}{2}}$ shows that it has been translated from a frequency that lies between the two adjacent bands. If the decimation and interpolation filters, $H_D(z)$ and $H_I(z)$, are designed such that $H_I(z)$ passes all of the frequency selectivity of $H_D(z)$ (i.e. the cascading of $H_D(z)$ and $H_I(z)$ yields an equivalent filter $H_D(z)$), then this system does approximate the equivalent system of Figure 3.4.

3.2.4 Filter design

Attention must now be turned to the design of the filters in the system. An advantage to using this architecture is the fact that there are only two digital filters in the system, which means only two sets of coefficients need to be stored. This is an advantage over most other perfect reconstruction filter banks, which often use a different filter design for each channel. The most critical design will be for $h_D[n]$ because it determines the performance of the system at the band edges. The lowpass frequency response of $H_D(f)$ is required to pass the band $\frac{-1}{2M} \leq f \leq \frac{1}{2M}$ (before the sample rate conversion) and stop everything else with a large amount of attenuation. Due to the fact that digital filters (or any filters, for that matter) cannot be designed to have zero transition bandwidth, it is assumed there is a finite transition bandwidth δ in the frequency response of $h_D[n]$ that needs to be preserved by $h_I[n]$ as shown in Figure 3.5. The interpolation filter therefore needs to have a passband edge which is above $\frac{1}{2M} + \frac{\delta}{2}$. After decimation by a factor of D and upsampling by a factor of 2, the required passband for the design of the interpolation filter becomes $|f| \geq \frac{D}{4M} + \frac{\delta D}{4}$. The upsampling also produces an undesired "copy" of the signal band centered at $f = \frac{1}{2}$. This copy must be eliminated by the interpolation filter. The requirements of the interpolation filter are that it must pass the desired term centered at $f = 0$ that covers the range of frequencies $\frac{-D}{4M} - \frac{\delta D}{4} \leq f \leq \frac{D}{4M} + \frac{\delta D}{4}$, and reject the aliased term centered at $f = \frac{1}{2}$ covering the range $\frac{1}{2} - (\frac{D}{4M} + \frac{\delta D}{4}) \leq f \leq \frac{1}{2} + (\frac{D}{4M} + \frac{\delta D}{4})$. Table 3.1 summarizes the passband and stopband edge requirements for the filter $h_I[n]$. The general case for decimation by D is given and the cases for $D = M$ and $D = \frac{M}{2}$ are evaluated for comparison. As stated in Section 3.2.2, the aliased terms overlap the edges of the desired signal for the case of maximal decimation, which is shown again in the values in the table for the passband and stopband edges of $h_I[n]$. The values for decimation by $D = \frac{M}{2}$ show the spacing between terms (provided that $\delta M < 1$) that eases the filter design. Figure 3.8 further

decimation rate	passband	stopband
D (general)	$\lvert f\rvert \leq \frac{D}{4M} + \frac{\delta D}{4}$	$\frac{1}{2} - (\frac{D}{4M} + \frac{\delta D}{4}) \leq f \leq \frac{1}{2} + \frac{D}{4M} + \frac{\delta D}{4}$
$D = M$	$\lvert f\rvert \leq \frac{1}{4} + \frac{\delta M}{4}$	$\frac{1}{4} - \frac{\delta M}{4} \leq f \leq \frac{3}{4} + \frac{\delta M}{4}$
$D = \frac{M}{2}$	$\lvert f\rvert \leq \frac{1}{8} + \frac{\delta M}{8}$	$\frac{3}{8} - \frac{\delta M}{8} \leq f \leq \frac{5}{8} + \frac{\delta M}{8}$

Table 3.1: Requirements of the interpolation filter for different rates of decimation

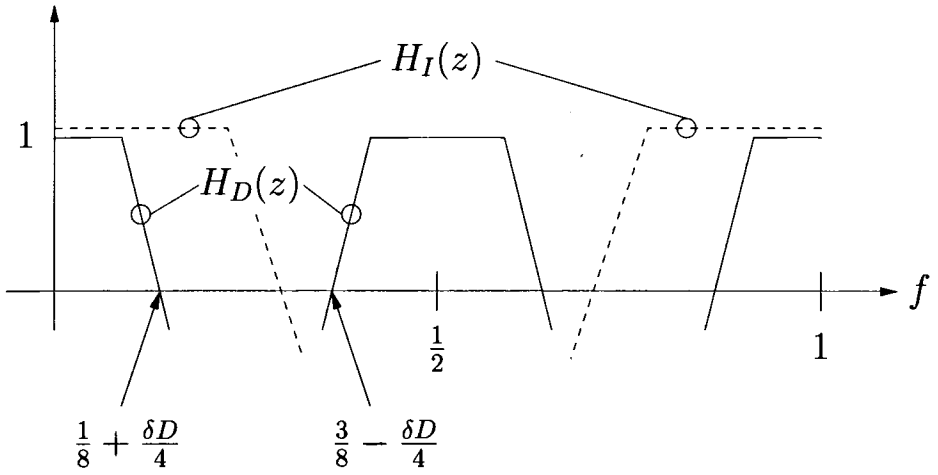
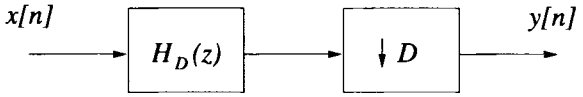
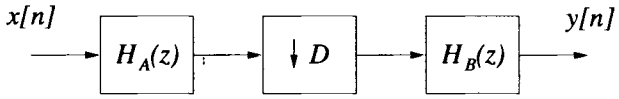


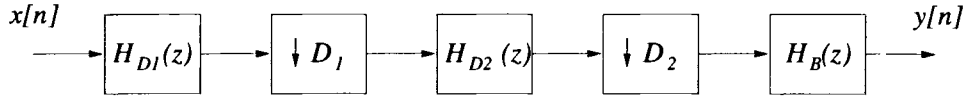
Figure 3.8: Requirements for interpolation filter $H_I(z)$ frequency response (for $D = \frac{M}{2}$)



(a) Single-stage decimation by D



(b) Multistage filtering of $H_D(z)$



(c) Two stage decimation by D

Figure 3.9: Multi-stage decimation and filtering

illustrates the filter requirements of $h_I[n]$ for the case $D = \frac{M}{2}$, where the upsampled terms that have been filtered by $h_D[n]$ are also shown.

The decimation filter $h_D[n]$ processes every channel with a lowpass response. Since it must be possible to recombine adjacent channels in the reconstruction, the filter $h_D[n]$ must have a symmetrical design. Due to the high decimation rate, designing filters with passbands that are small relative to the sampling frequency is difficult. Designing these filters with tight specifications in the transition band is even more difficult because the transition band is also small.

3.2.4.1 Multistage decimation

The steps in the design process of the filter $H_D(z)$ are illustrated in Figure 3.9, where the straightforward approach to decimation by D is shown in Figure 3.9(a). The filter design can be simplified if it can be done at a lower sampling rate where the passband and the transition band δ take up a larger part of the sampling bandwidth.

By breaking the filter $h_D[n]$ into two separate filters with one filter each used to process the signal before and after decimation, the design becomes much easier. This method, shown in Figure 3.9(b), divides the responsibilities of the decimation filter between the two new filters, $H_A(z)$ and $H_B(z)$. The filter $H_A(z)$ that precedes the down-sampling is used to remove any signal components that may alias into the particular band of interest. This filter design focuses on the location of stopbands rather than the symmetric passband edges, which is not a difficult design if the decimation rate is fairly low.

For higher decimation rates the act of down-sampling is often performed by cascading filter and decimation blocks, a technique that is illustrated in Figure 3.9(c). The filter $H_A(z)$ and the decimation by D has been split into two new stages composed of filters $H_{D1}(z)$ and $H_{D2}(z)$ and decimation by factors of D_1 and D_2 (where $D_1 D_2 = D$). The complexity of the filter in each stage is reduced by the following stage because the number of aliased bands that must be filtered out at each stage decreases as the number of stages increases. The spacing between these aliased bands therefore increases with the number of decimation stages, which also makes the designs for $H_{D1}(z)$ and $H_{D2}(z)$ easier [6].

The filter $H_B(z)$ at the end of the decimation stage in Figures 3.9(b) and 3.9(c) provides the symmetric edges for recombination. This filter is always implemented at the lowest sampling rate in the two-channel stage, which makes it a much simpler design than the original solution of using a single filter.

3.2.4.2 Half-band filters

As previously stated, in order to recombine the signals from two neighboring bands, the filter $H_D(z)$ should have symmetric edges. For a decimation rate of $D = \frac{M}{2}$ the filtered signal $\hat{x}_k[n]$ covers the range $|f| \leq \frac{1}{4} + \frac{\delta M}{4}$. The filter $H_D(z)$ must then have symmetric edges about the frequency $f = \frac{1}{4}$ so that the two signals $\hat{x}_k[n]$ and $\hat{x}_{k+1}[n]$ will add together correctly at the band edges. The transition band $\frac{\delta M}{2}$ should extend

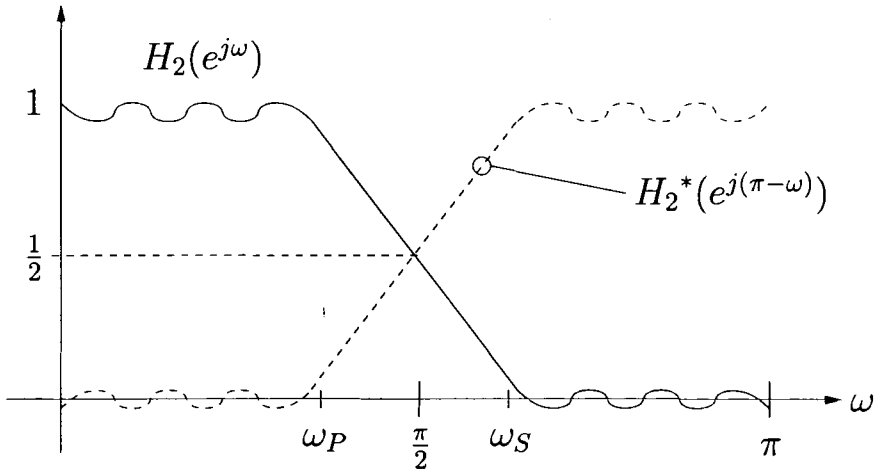


Figure 3.10: Frequency response of a half-band filter

equally into the passband and stopband. The filter bank composed of the two filters represented by the terms $H_D(z^{2/D}W_M^{1/2})$ and $H_D(z^{2/D}W_M^{-1/2})$ from (3.21) should be some form of complimentary filter bank. A delay-complimentary filter bank is classified as

$$\sum_{\gamma=0}^{M-1} H_\gamma(z) = \beta z^\alpha \qquad \beta \neq 0 \tag{3.22}$$

where the filters $H_\gamma(z)$ compose the M-channel filter bank [6]. The filters of a delay-complimentary bank add together to pass the entire sampled bandwidth.

A set of filters called half-band filters meet the above requirements of being symmetric and complimentary. These filters are part of the class of Lth-band filters, which are characterized by having a zero at every Lth coefficient in its impulse response. The term at the origin is a constant, and these requirements are given in the standard equation for even order Lth band filters:

$$h_L[nL] = \begin{cases} \alpha, & n = 0, \\ 0, & \text{otherwise.} \end{cases} \tag{3.23}$$

Half-band filters are Lth band filters where $L = 2$ and $\alpha = \frac{1}{2}$. Since every even indexed coefficient except for $h_2[0]$ is zero, the polyphase decomposition of $H_2(z)$ yields

$$H_2(z) = \frac{1}{2} + z^{-1}E_1(z^2) \tag{3.24}$$

where $E_1(z)$ is the first polyphase component of $H_2(z)$, and the polyphase components of an Lth band filter are found by

$$E_k(z) = \sum_{n=0}^{\infty} h_L[k + nL]z^{-n} \qquad 0 \leq k \leq L - 1. \tag{3.25}$$

The relation given in (3.24) can be reduced to

$$H_2(z) + H_2(-z) = 1. \tag{3.26}$$

If $h_2[n]$ has real coefficients, then $H_2(-e^{j\omega}) = H_2{}^*(e^{j(\pi-\omega)})$, and (3.26) gives

$$H_2(e^{j\omega}) + H_2{}^*(e^{j(\pi-\omega)}) = 1. \tag{3.27}$$

This equality shows that the half-band filter exhibits symmetry about the quadrature frequency $\omega = 2\pi\left(\frac{1}{4}\right) = \frac{\pi}{2}$ as shown in Figure 3.10. It also shows that the two filters in (3.27) are complimentary. The passband and stopband edges are symmetric with respect to $\omega = \frac{\pi}{2}$, meaning that $\omega_p + \omega_s = \pi$ and $\omega_s - \omega_p = \delta$. The filter also has equal passband and stopband ripple [6].

Half-band filters only pass the first half of the sampling bandwidth centered at $f = 0$. The half-band filter is used to set the final signal bandwidth for the channel as shown in Figure 3.7, where for the case $D = \frac{M}{2}$, the $i = 0$ term covers the range $|f| \leq \frac{1}{4}$, which corresponds to the passband of the half-band filter. The edges of two half-band filters operating on opposite halves of the spectrum add up to a constant across

the transition band, as shown by (3.27). This property is desired of the filter $H_D(z)$, and since the last filter in Figure 3.9(c) sets the transition band characteristic, the filter $H_B(z)$ is chosen to be a half-band filter.

3.2.5 Signal delay

The linear phase filters used in this design all impose different sample delays on the signal as it moves through the system. As the signals are modulated in the recombination block, terms are generated that alter the phase of the signals. These terms are scale factors that must be corrected in order to assure that the entire system is linear phase and does not distort the group delay of the signal. A causal filter has linear phase if its impulse response is either symmetric or antisymmetric [6]. Filters that display symmetry can be represented in the form

$$H(z) = z^{-l} H_R(z) \tag{3.28}$$

where l respresents a unit sample delay and $H_R(z)$ is the real-valued amplitude response of the filter. For a filter of order N (either symmetric or antisymmetric) that has $N+1$ coefficients, the value of l is given by

$$l = \frac{N}{2}. \tag{3.29}$$

As linear phase filters, $h_D[n]$ and $h_I[n]$ can be decomposed as in (3.28) to yield

$$\begin{aligned} H_D(z) &= z^{-l_1} H_{DR}(z) \\ H_I(z) &= z^{-l_2} H_{IR}(z). \end{aligned} \tag{3.30}$$

The changes in the phase of the signal as it is processed by the system can be found by substituting (3.30) into (3.19) to find

$$\begin{aligned} A_k(z) &= \frac{1}{D} z^{-l_2} e^{-j\frac{\pi l_2}{4}} H_{IR}(ze^{j\frac{\pi}{4}}) z^{\frac{-2l_1}{D}} W_M^{\frac{l_1}{2}} H_{DR}(z^{2/D} W_M^{-1/2}) X(z^{2/D} W_M^{-(k+\frac{1}{2})}) \\ &= \frac{1}{D} H_{IR}(zW_M^{-D/4}) H_{DR}(z^{2/D} W_M^{-1/2}) X(z^{2/D} W_M^{-(k+\frac{1}{2})}) z^{-d_{k:k+1}} W_M^{c_{k:k+1}} \end{aligned} \tag{3.31}$$

where the cofficients $d_{k:k+1}$ and $c_{k:k+1}$ are given by

$$\begin{aligned} d_{k:k+1} &= \frac{2l_1}{D} + l_2 \\ c_{k:k+1} &= \frac{l_1}{2} + \frac{l_2 D}{4}. \end{aligned} \tag{3.32}$$

Similarly, the signal in the opposite channel is found using (3.20) to be

$$A_{k+1}(z) = \frac{1}{D} H_{IR}(zW_M^{D/4}) H_{DR}(z^{2/D} W_M^{1/2}) X(z^{2/D} W_M^{-(k-\frac{1}{2})}) z^{-d_{k:k+1}} W_M^{-c_{k:k+1}}. \tag{3.33}$$

The phase shift $W_M^{c_{k:k+1}}$ needs to be corrected in each stage in order to maintain a linear phase characteristic to give the phase corrected recombined output. The signal $\tilde{y}_{k:k+1}[n]$ becomes

$$\tilde{Y}_{k:k+1}(z) = A_k(z) W_M^{-c_{k:k+1}} + A_{k+1}(z) W_M^{c_{k:k+1}}. \tag{3.34}$$

The delay term that is left, $z^{-d_{k:k+1}}$, will produce phase shift terms in the next stage.

All the recombination blocks are identical to that shown in Figure 3.3. For the second stage, the inputs $\tilde{y}_{k:k+1}[n]$ and $\tilde{y}_{k+2:k+3}[n]$ are recombined to give $\tilde{y}_{k:k+3}[n]$. The signal $a_{k:k+1}[n]$ produced from the input $\tilde{y}_{k:k+1}[n]$ is given by

$$A_{k:k+1}(z) = z^{-l_2} e^{-j\frac{\pi l_2}{4}} H_{IR}(zW_M^{-D/4}) \tilde{Y}_{k:k+1}(z^2 e^{j\frac{\pi}{2}}). \tag{3.35}$$

stage	# bands	coefficient	coefficient formula	factor
1	2	$c_{k:k+1}$	$\frac{l_1}{2} + \frac{l_2 D}{4}$	$W_M^{\pm c_{k:k+1}}$
2	4	$c_{k:k+3}$	$l_1 + \frac{3l_2 D}{4} = 2c_{k:k+1} + \frac{l_2 D}{4}$	$W_M^{\pm c_{k:k+3}}$
3	8	$c_{k:k+7}$	$2l_1 + \frac{7l_2 D}{4} = 2c_{k:k+3} + \frac{l_2 D}{4}$	$W_M^{\pm c_{k:k+7}}$
4	16	$c_{k:k+15}$	$4l_1 + \frac{15l_2 D}{4} = 2c_{k:k+7} + \frac{l_2 D}{4}$	$W_M^{\pm c_{k:k+15}}$

Table 3.2: Phase shift factor coefficients for 4 stages of an M-channel system

Substitution of (3.31) through (3.34) into (3.35) yields new delay and phase shift terms

$$\begin{aligned} d_{k:k+3} &= \frac{4l_1}{D} + 3l_2 \\ &= 2d_{k:k+1} + l_2 \\ c_{k:k+3} &= l_1 + \frac{3l_2 D}{4} \\ &= 2c_{k:k+1} + \frac{l_2 D}{4} \end{aligned} \tag{3.36}$$

where the old delay and phase shift coefficients have been doubled by the interpolation step, and an additional amount of delay and phase shift is put on the signal by the filter $h_I[n]$ in every recombination stage. The second stage output $\tilde{y}_{k:k+3}[n]$ is found as in (3.34) using the new phase shift factors

$$\tilde{Y}_{k:k+3}(z) = A_{k:k+1}(z) W_M^{-c_{k:k+3}} + A_{k+2:k+3}(z) W_M^{c_{k:k+3}}. \tag{3.37}$$

The generation of these phase shift correction factors is an iterative process through the system, and corrections must be made at the output of every stage. Factors for the first four stages of a system using decimation of $D = \frac{M}{2}$ are given in Table 3.2. It should be noted that factors generated from recombining the same number of bands are equal, for example

$$c_{k:k+3} = c_{k+4:k+7} = c_{k+6:k+9} \tag{3.38}$$

where all of the factors are generated from the recombination of 4 signal bands.

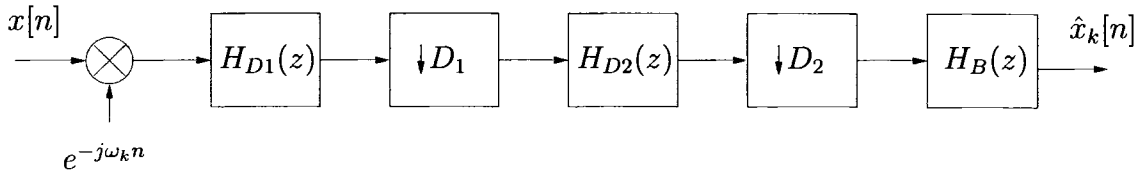


Figure 3.11: Final channel decimation block design

3.3 Filter bank design summary

The final design for the recombination filter bank includes all of the parts discussed in Section 3.2. The design for the decimation and filtering in each channel prior to recombination appears in Figure 3.11. The decimation filter is implemented in two parts, where the first filter selects the proper frequency range to pass by eliminating any signals that may alias onto the desired signal during the decimation. This filter, along with the decimation block, is implemented in two stages composed of filters $H_{D1}(z)$ and $H_{D2}(z)$ and decimation by D_1 and D_2. The two stage decimation makes filter design easier than a single stage decimation. The second part of the decimation filter, the half-band filter $H_B(z)$, sets the transition band of the filtering process so the band edges will line up when the signals are recombined.

The final design for the recombination block is shown in Figure 3.12. The upsampling block and the interpolation filter $H_I(z)$ increase the sample rate by a factor of two. The signal in each channel is then modulated in oppostie directions to be recombined. The phase correction factors are applied after modulation in each channel with opposite signs on each exponential. The signals are then added together to complete the recombination step. Specific digital filter designs are given in the next chapter.

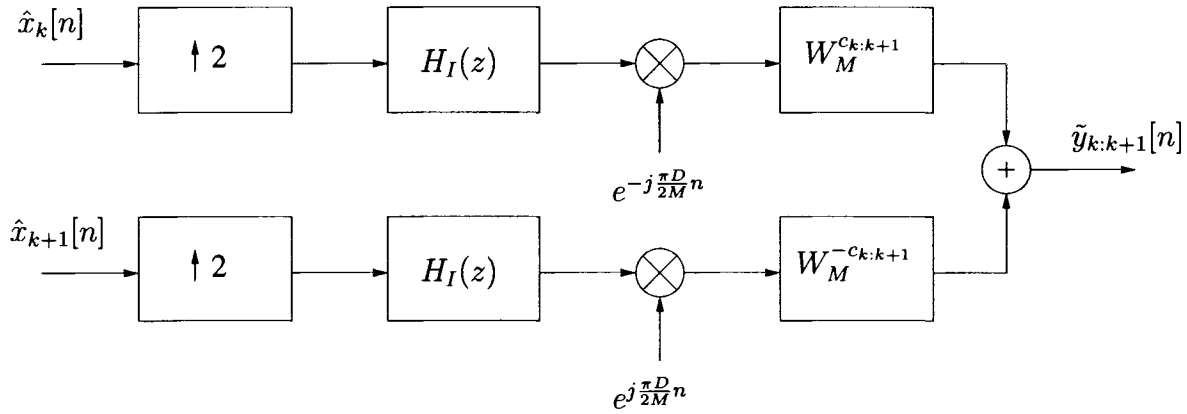


Figure 3.12: Final recombination block design

CHAPTER 4

ARCHITECTURE DESIGN

This chapter shows the design of a recombination filter bank for use with $\Sigma\Delta$ ADCs. The specifications for the data converters that govern architecture design are discussed, and the decimation and interpolation filter designs are given. The recombination performance of the filter bank is examined through MATLAB simulation, and finally the architecture is simulated with $\Sigma\Delta$ sampling modules.

4.1 Channel ADCs

This particular design uses $\Sigma\Delta$ ADCs to quantize the subband signal in each channel. This allows each band of frequencies to be quantized with a high degree of resolution. The end result is that the noise-shaping effect of the $\Sigma\Delta$ ADC appears in each band across the first Nyquist Band.

4.1.1 Frequency selective IQ $\Sigma\Delta$ ADC

The $\Sigma\Delta$ architecture simulated in this design example is modeled after the frequency selective IQ $\Sigma\Delta$ ADC circuit designed and constructed in [1]. This device implements the modulators and ADCs all in one package. In-phase and quadrature channels are used to produce complex samples of the bandpass representation of the signal in each band. The prototype built in [1] used a fourth-order multistage noise shaping (MASH) architecture composed of two cascaded second-order loops in each channel, although for the purposes of this simulation, different order loops are used to model the ADC. The oversampling rate (OSR) is 32, and the modulators are configured to select one of 16 bands across the first Nyquist band for quantization.

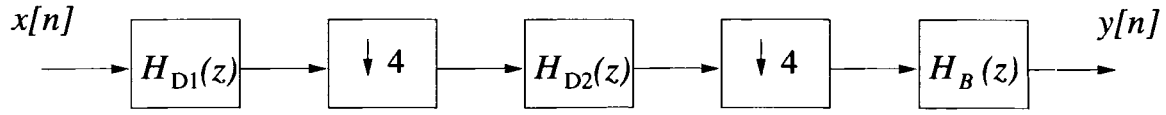


Figure 4.1: Cascaded downsamplers to achieve decimation by 16

4.1.2 Division of channels

The useable bandwidth of a $\Sigma\Delta$ ADC is normally given to be $\frac{F_s}{\text{OSR}}$, so this sets the bandwidth of each channel in the system. One IQ $\Sigma\Delta$ structure is used to quantize the information in each band. The bands are divided as shown in Figure 2.8, which illustrates the case for $M = 16$ where the first 8 channels are to be quantized and reconstructed. In order to model the hardware, this simulation has 32 channels, and the first 16 channels are to be recombined. Each subband signal has a bandwidth of $B = \frac{1}{M}$, and each band is centered at $f_k = \frac{k}{M}$ for $k = 0, 1, 2, ...15$. Each channel prepares the subband signal for recombination using a relaxed decimation of $D = \frac{M}{2} = 16$.

4.2 Filter designs

Linear phase filters are used in this design in order to preserve the group delay of the input signal. The amplitude information is kept intact by designing the filters to provide enough attenuation to the signals outside the band of interest, as well as using a symmetrical design for the decimation filter so that adjacent band edges will add correctly.

4.2.1 Decimation filtering

The filter designs $h_D[n]$ and $h_I[n]$ are critical to the performance of the system. The passband ripple of both filters should be low so that the desired signal is not distorted, and the stopband attenuation should be high to prevent the aliasing of unwanted

terms. For these reasons the filters are designed to have a maximum passband ripple of 0.1 dB and a minimum stopband attenuation of at least 100 dB.

The design of the decimation filter $h_D[n]$ shows that a high OSR can make the filter design quite difficult. For OSR $= 32$, Figure 3.5 shows that the required filter has a lowpass characteristic with a passband edge frequency of $f_p = \frac{1}{64} - \frac{\delta}{2}$ and a stopband edge frequency of $f_s = \frac{1}{64} + \frac{\delta}{2}$. This is a very difficult filter to implement and requires a large number of coefficients. The filter design can be simplified as described in Section 3.2.4 by using multiple decimation stages and implementing the critical filter at the lowest sampling rate. For this design, decimation by $D = 16$ is achieved by cascading two sections of decimation by $D_1 = D_2 = 4$ as in Figure 4.1. The filters $h_{D1}[n]$, $h_{D2}[n]$, and $h_B[n]$ are then designed as outlined in Section 3.2.4, where the maximum passband ripple has been divided among the three filters (each filter is allowed 0.0333 dB passband ripple). The stopband attenuation is still a minimum of 100 dB for all filters because each one attenuates different aliased terms.

The designs are very similar for filters $h_{D1}[n]$ and $h_{D2}[n]$ because both filters prepare the signal for decimation by 4. The decimation stretches the frequency axis, and so any signals that may be translated to a multiple of $f = 1$ will alias onto the desired lowpass signal. The three areas that alias onto the desired signal are located at $f = \frac{1}{4}$, $f = \frac{1}{2}$, and $f = \frac{3}{4}$. The passband requirements for the two filters as outlined above appear in Figure 4.2. The two filters have stopbands in the same regions because of the equal decimation rates, although the regions have different widths because the filters operate at different sample rates.

Due to the regions of the frequency response that have no specifications, the designs for these filters lend themselves to the Remez exchange algorithm [6]. This procedure uses an iterative process to minimize the error between a possible solution and the desired response in different bands of frequencies. The response of the filter in the regions that are not specified by the user is designed by the algorithm. The iterations

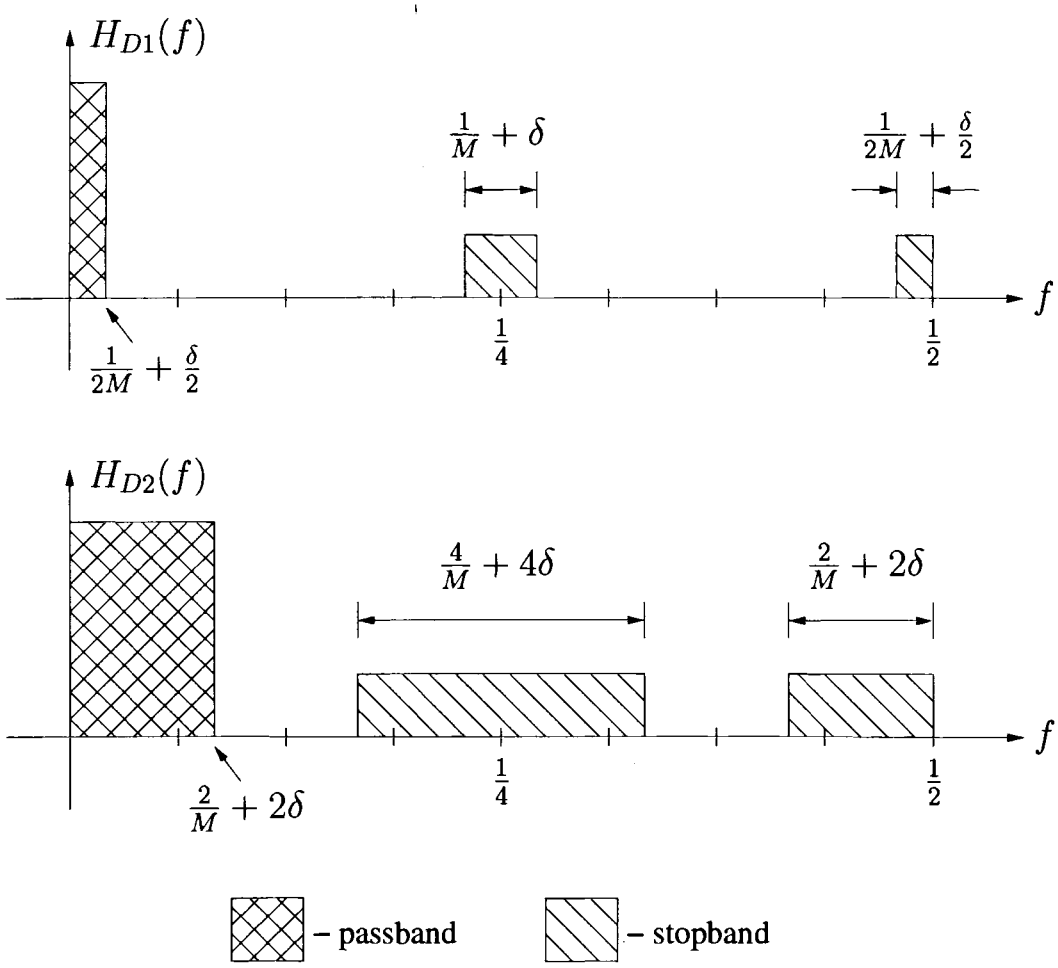
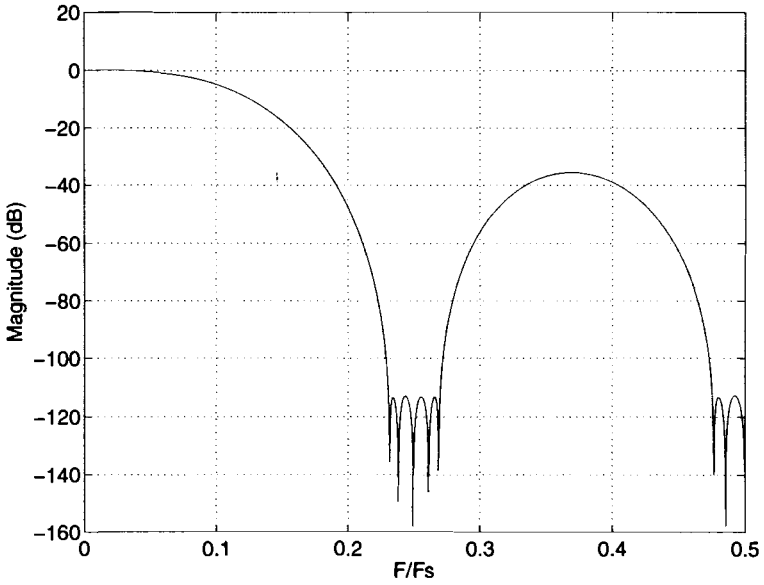
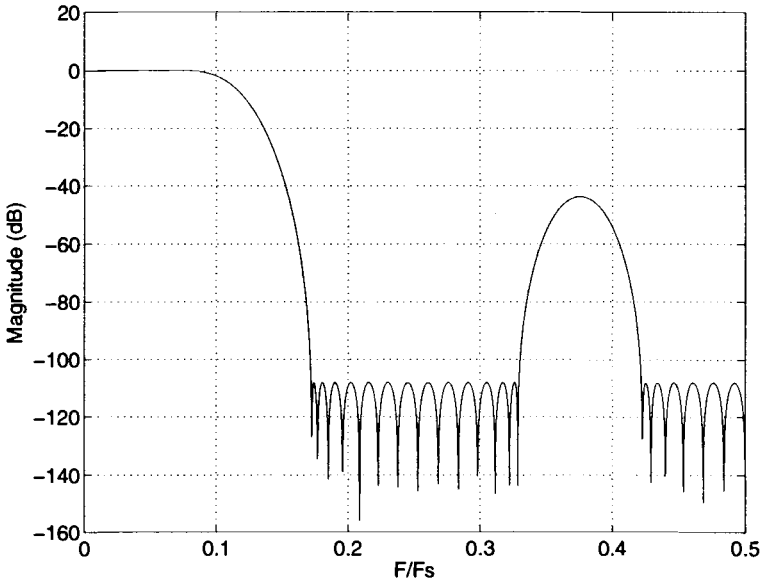


Figure 4.2: Passband and stopband requirements for decimation filters $h_{D1}[n]$ and $h_{D2}[n]$



(a) First decimation filter $H_{D1}(z)$



(b) Second decimation filter $H_{D2}(z)$

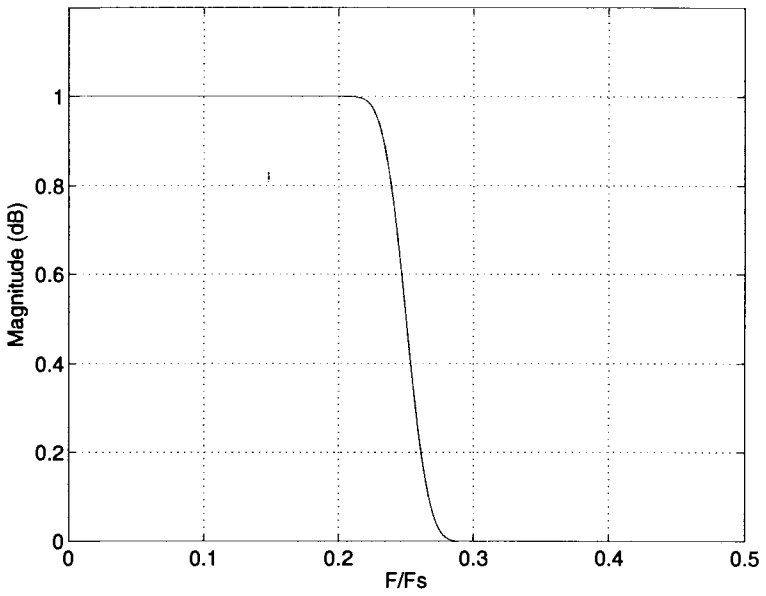
Figure 4.3: Frequency responses of decimation filters

end once the error falls below a certain threshhold, and the number of coefficients is adjusted until the filter specifications are met. The Remez exchange algorithm was used to design the filters $h_{D1}[n]$ and $h_{D2}[n]$ whose frequency responses appear in Figure 4.3. The passbands of $h_{D1}[n]$ and $h_{D2}[n]$ are designed to include signals that will be shaped by the transition band of $h_B[n]$, and so a tolerance of $\delta = 0.5(\frac{1}{2M})$ was used in the designs of $h_{D1}[n]$ and $h_{D2}[n]$. Filter $h_{D1}[n]$ was designed using 18 coefficients while $h_{D2}[n]$ was designed with 52 coefficients. These linear phase filters have symmetric impulse responses, so only half of the coefficients of each filter need to be stored in memory.

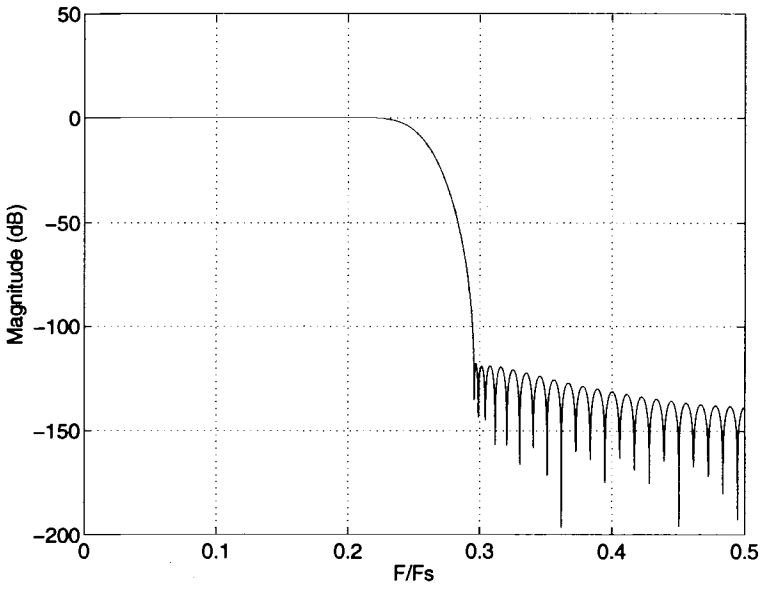
The final decimation filter $h_B[n]$ was designed as a half-band filter using the windowed Fourier series approach [6]. This method uses the windowed version of the Fourier transform of an ideal filter response to create a linear phase filter that approaches the desired response based on the number of coefficients used. This particular half-band filter was designed with a Kaiser window using 84 coefficients, and its frequency response appears in Figure 4.4. The frequency response is plotted on both linear and logarithmic scales so that the symmetry of the filter can be seen. The tolerance used in the designs of $h_{D1}[n]$ and $h_{D2}[n]$ is adequate for this design of $h_B[n]$ as its stopband begins before $f = 0.3$, whereas the two decimation filters are designed to allow a stopband frequency as high as

$$\begin{aligned} D\left(\frac{1}{2M}+\frac{\delta}{2}\right) &= \frac{M}{2}\left(\frac{1}{2M}+\frac{1}{8M}\right) \\ &= \frac{1}{4}+\frac{1}{16} \\ &= 0.3125. \end{aligned} \tag{4.1}$$

The symmetric frequency response of the filter dictates that the passband and stopband ripple of the filter are equal, which results in an unusually small passband ripple when high stopband attenuation is needed. This symmetry means that only about half of the



(a) Frequency response of half-band filter (linear scale)



(b) Frequency response of half-band filter (dB scale)

Figure 4.4: Frequency response of decimation filter $h_B[n]$

coefficients need to be stored in memory, although, as stated earlier, nearly half of the coefficients for a half-band filter are zero. This means that roughly a quarter of the filter coefficients are unique and need to be stored in memory.

Each decimation filter applies a different delay to the signal as described in Section 3.2.5, although the delay term z^{-l_1} is now distributed among three different filters at three different sample rates. The first decimation $h_{D1}[n]$ filter is of order 17, and using (3.29) is found to impose a delay of $l_{11} = 8.5$ samples on the signal. Similarly, the other two decimation filters $h_{D2}[n]$ and $h_B[n]$ delay the signal by $l_{12} = 25.5$ and $l_{13} = 42$ samples, respectively. However, the sample rate is decimated by a factor of 4 after the first filter, which has the effect of stretching the frequency axis. The second decimation filter therefore appears 4 times longer than it actually is to the signal. A delay of $4l_{12} = 102$ samples is imposed by the second filter, and the third filter delays the signal by $16l_{13} = 672$ samples. The equivalent delay of the three decimation filters is then the sum of the delays imposed by each of the filters,

$$l_1 = l_{11} + 4l_{12} + 16l_{13} = 782.5. \tag{4.2}$$

4.2.2 Interpolation filtering

The interpolation filter is the simplest of all the filter designs as there is only one passband and one stopband with a wide transition band. The maximum passband ripple is set at 0.1 dB and the minimum stopband attenuation at 100 dB following the same reasoning used in the design of the decimation filter. A gain of two was also included in the passband of the filter to maintain amplitude throughout the interpolation step. When the sample rate is increased by two, the energy in the signal remains the same, although it is spread out over twice as many samples. The system only uses half of this spectral bandwidth, and so amplification is needed to preserve the original signal strength.

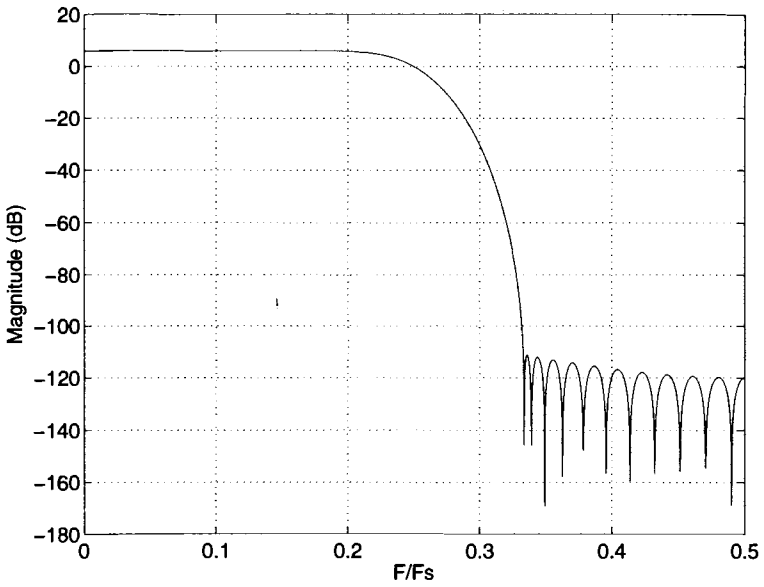


Figure 4.5: Frequency response of interpolation filter $h_I[n]$

The two methods used in the design of the decimation filters were attempted in the implementation of the interpolation filter. The Remez exchange algorithm produces a filter that met the specifications shown in Figure 3.8, although a half-band filter design with the same specifications needs fewer coefficients stored in memory to construct the same filter. The frequency response of the half-band interpolation filter designed using 47 coefficients is shown in Figure 4.5. This filter imposes a delay of $l_2 = 23.5$ samples on the signal, and has a gain of 6 dB in the passband.

The filter designs for the recombination filter bank are summarized in Table 4.1. The use of half-band filters greatly reduces the number of coefficients that must be stored in memory, as does the fact that these 4 filters are the only filters needed by

filter	order	num. coefficients	passband ripple (dB)	stopband attenuation (dB)
$h_{D1}[n]$	17	9	0.016	112
$h_{D2}[n]$	51	26	0.028	107
$h_B[n]$	84	22	2.6E-5	117
$h_I[n]$	46	13	3.8E-5	111

Table 4.1: Filter specifications

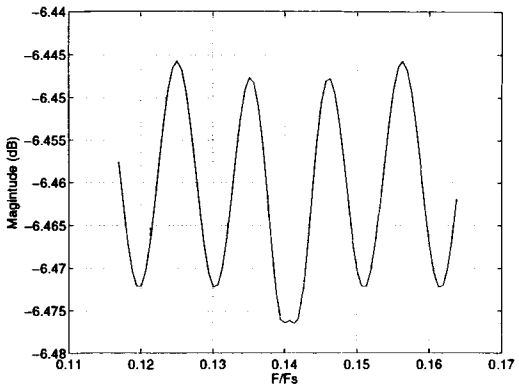
the system to recombine up to 16 channels. All of the filters have enough stopband attenuation to eliminate out-of-band terms that may alias onto the desired signal. The anticipated passband distortion of the overall structure has been reduced by using half-band filters as well. Filters $h_{D1}[n]$ and $h_{D2}[n]$ approach the allowed passband ripple figure of 0.0333 dB, but the passband ripple of filter $h_B[n]$ is a few orders of magnitude below this amount due to the symmetry of the filter. The same can be said of the interpolation filter $h_I[n]$, which meets the minimum stopband requirement of 0.1 dB again by a few orders of magnitude. The values $l_1 = 782.5$ and $l_2 = 23.5$ are used in the calculation of the phase-shift correction factors in every recombination stage as outlined in Section 3.2.5.

4.3 Recombination performance

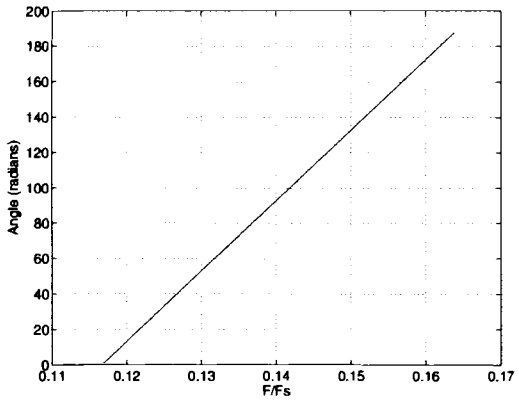
The recombination performance of the filter bank is now evaluated. The MATLAB simulation of the recombination of several bands of frequencies is discussed, and the results are examined.

4.3.1 Filter bank performance

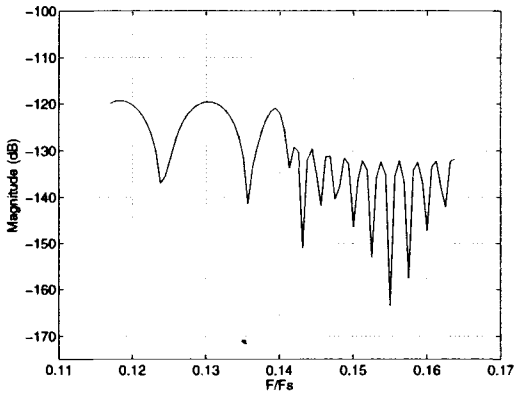
The filter bank is first tested using a single frequency test signal that is swept across the neighboring bands that are to be recombined. An amplitude of 0.95 V and a randomly selected phase are used at all frequencies of the test. The signal at the output of the recombination block is examined for amplitude and phase distortion. The single-tone test gives a good indication of how well the system handles aliased terms, as the only signal that should appear at the output is the test signal. The following simulations show the recombination of 2, 4, and 16 channels.



(a) Signal amplitude



(b) Signal phase



(c) Peak distortion

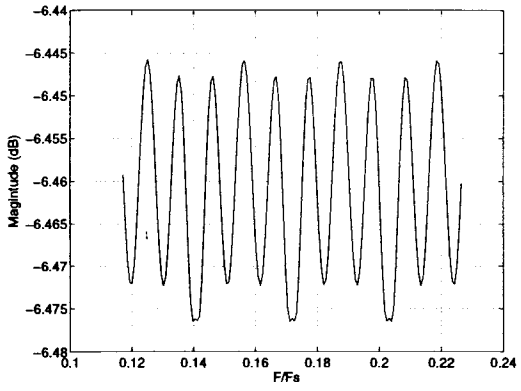
Figure 4.6: Measurements for recombination of bands 4 and 5

Two band reconstruction

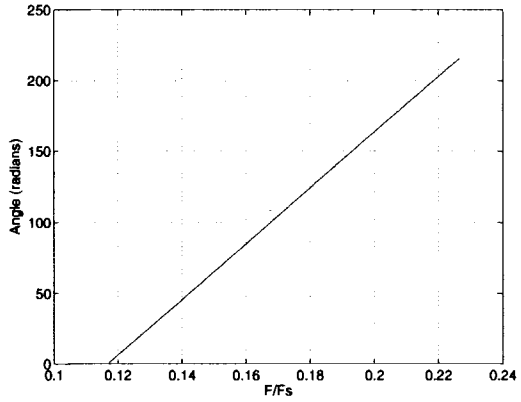
Results for the two band recombination test are shown in Figure 4.6. Figure 4.6(a) shows the amplitude of the output signal as it is marched across the $k = 4$ and $k = 5$ bands. For a signal amplitude of 0.95 V, only half that power would fall in the first Nyquist band, which corresponds to -6.466 dBv of power. The signal power measured at the output of the recombination block varies by less than 0.04 dB around this value, even in the middle of the figure where the band edges meet. The phase of the output signal is illustrated in Figure 4.6(b), where it can be seen that the system is linear phase and thus does not introduce any delay distortion. The maximum peak other than the test signal for each test frequency appears in Figure 4.6(c). The peak distortion is well below -100 dB at all test frequencies, which indicates that aliased terms have been well attenuated across the two bands. These results show that the system has approximated a perfect reconstruction in the recombination of two bands.

Four band reconstruction

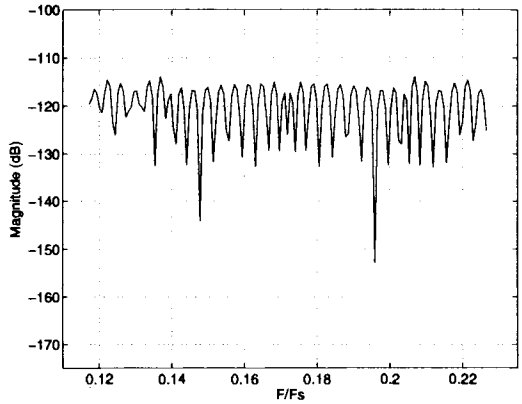
Results for the recombination of bands $k = 4$ through $k = 7$ appear in Figure 4.7. The testing procedure is the same as for two bands except now the test signal is swept across four bands. These results are similar to those seen in the previous case. The amplitude distortion shown in Figure 4.6(a) has not increased from the case for two bands, and the phase characteristic is still linear, as shown in Figure 4.6(b). The peak distortion curve in Figure 4.6(c) has a more uniform shape than that for the previous case, although the peak values have not increased. These results confirm that additional channels can be recombined with the same accuracy of the two band case simply by cascading recombination blocks.



(a) Signal amplitude

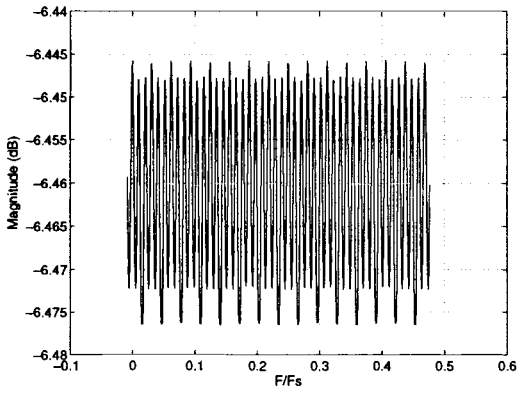


(b) Signal phase

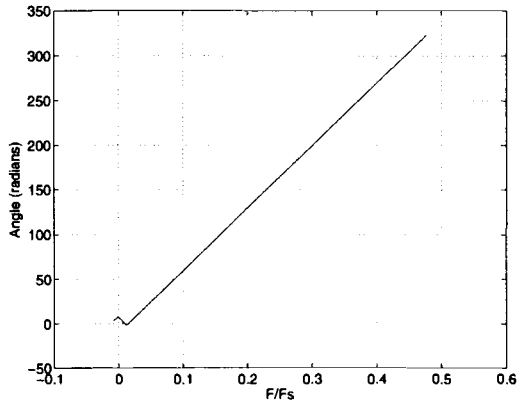


(c) Peak distortion

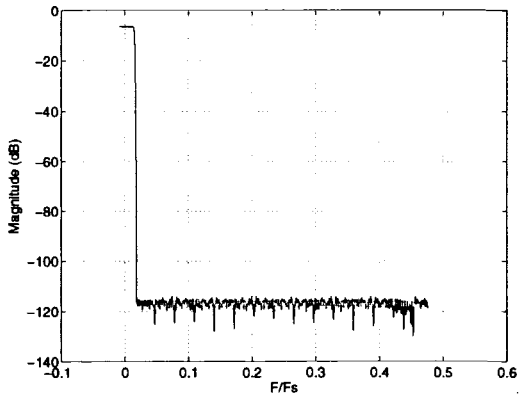
Figure 4.7: Measurements for recombination of bands 4 through 7



(a) Signal amplitude



(b) Signal phase



(c) Peak distortion

Figure 4.8: Measurements for recombination of bands 0 through 15

16 band reconstruction

The measurements for the recombination of 16 bands (bands $k = 0$ through $k = 15$) is illustrated in Figure 4.8. The curve in Figure 4.8(a) remains bounded between the same limits as the previous two cases, which provides further evidence that the structure is capable of reconstructing wide bandwidth signals. The phase and peak distortion curves shown in Figures 4.8(b) and 4.8(c) both display behavior that deviates from the expected results near the origin. This phenomenon can best be explained by examining the peak distortion curve of Figure 4.8(c). When the test signal is within the frequency range of the first band (for $k = 0$), the mirror image from the second Nyquist band is in the negative range of frequencies that falls in the same band. When one of the tones is considered to be the signal, the other tone is considered to be the peak distortion by the simulation. Once the signal passes through the $k = 0$ band, so does its conjugate image signal. The same phenomenon occurs for test signals in bands that are multiples of the number of channels ($M = 32$ in this case). When the signal is in this range of frequencies, either tone may be taken as the signal as they move through the filters. This appears to explain the phase plot of Figure 4.8(b), as the simulation alternates between the two baseband tones and is actually measuring the phase of two different signals. The system performs as expected across all other bands.

This phenomenon can be alleviated by filtering out the tone from the second Nyquist band. This can be accomplished using a Hilbert transfomer, which is a complex-valued filter that attenuates negative frequencies while passing positive frequencies [6]. The frequency response of the Hilbert transformer appears in Figure 4.9. This filter is merely a halfband filter that has been frequency translated by $\frac{\pi}{2}$. This eliminates the need for another filter design as the Hilbert transformer can be generated from the previously designed half-band filter $h_B[n]$. The Hilbert transformer $g_H[n]$ is generated by the modulation

$$g_H[n] = h_B[n]e^{j\frac{\pi n}{2}}. \tag{4.3}$$

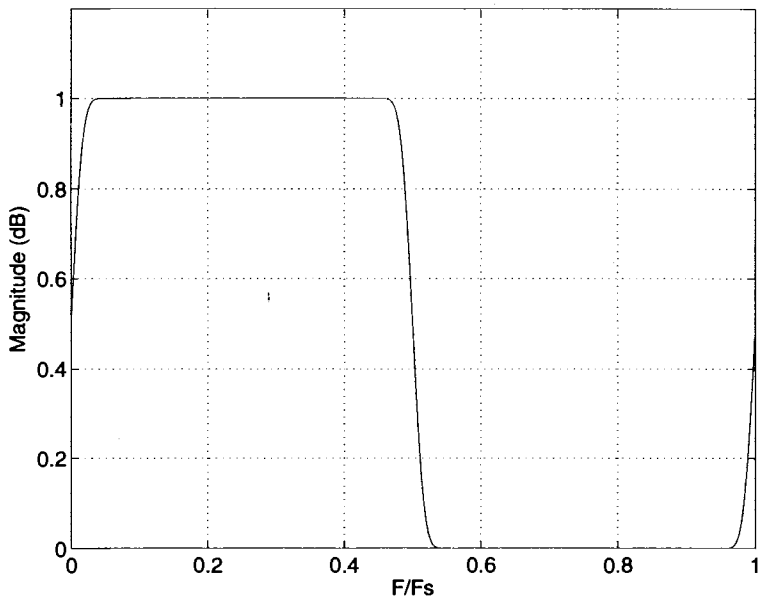
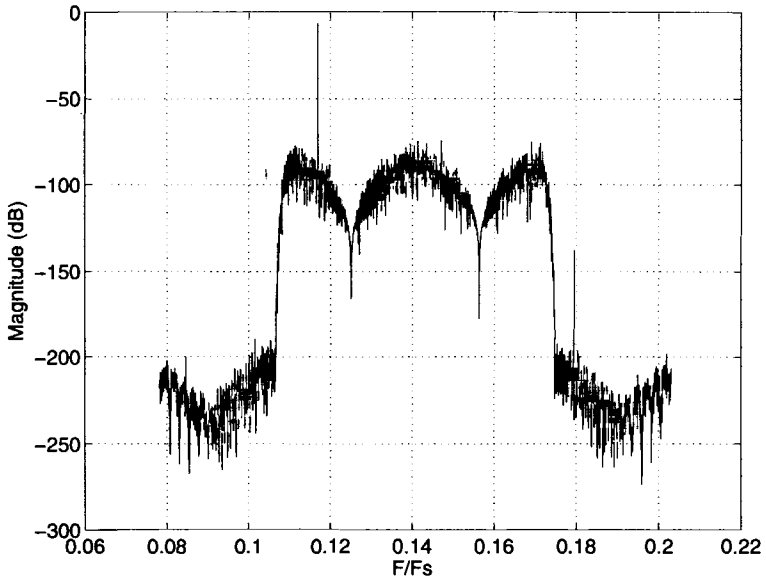


Figure 4.9: Frequency response of a Hilbert transformer

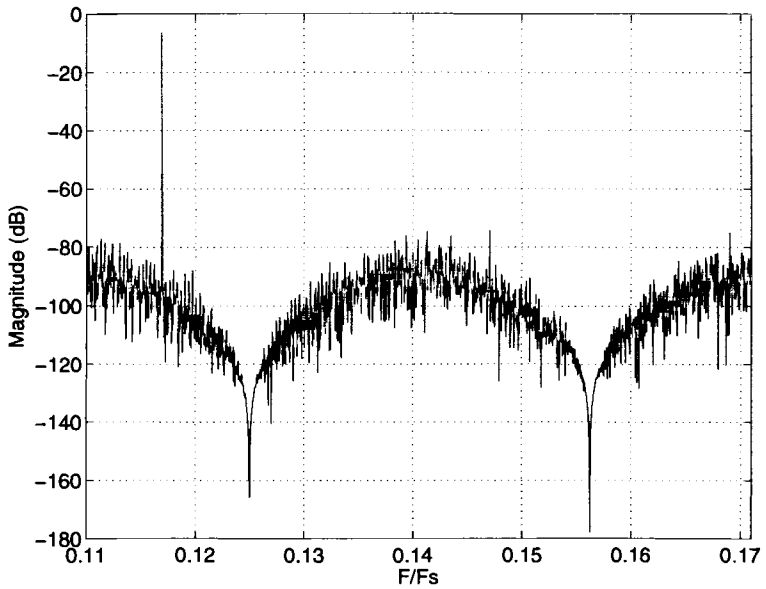
The Hilbert transformer can be included in the decimation filter $h_D[n]$ of the sampling module that operates on the $k = 0$ band.

4.3.2 Sampling architecture performance

The true test of the architecture includes the full sampling modules complete with IQ $\Sigma\Delta$ ADC structure in each channel. The sampling modules are modelled after the prototype designed in [1], and as such consist of in-phase and quadrature channels as in Figure 2.5 with $\Sigma\Delta$ ADCs as the channel quantizers. There are no lowpass filters preceding the data converters because the noise-shaping of the $\Sigma\Delta$ acts as a lowpass filter in that higher frequency signals are lost in the quantization noise. The lowpass decimation filter $h_D[n]$ and down-sampling block complete the sampling module. The quantizers are as outlined in Section 4.1.



(a) Second order $\Sigma\Delta$ recombination



(b) Close up of Figure 4.10(a)

Figure 4.10: Single-tone test in bands 4 and 5

Single-tone 2 band test

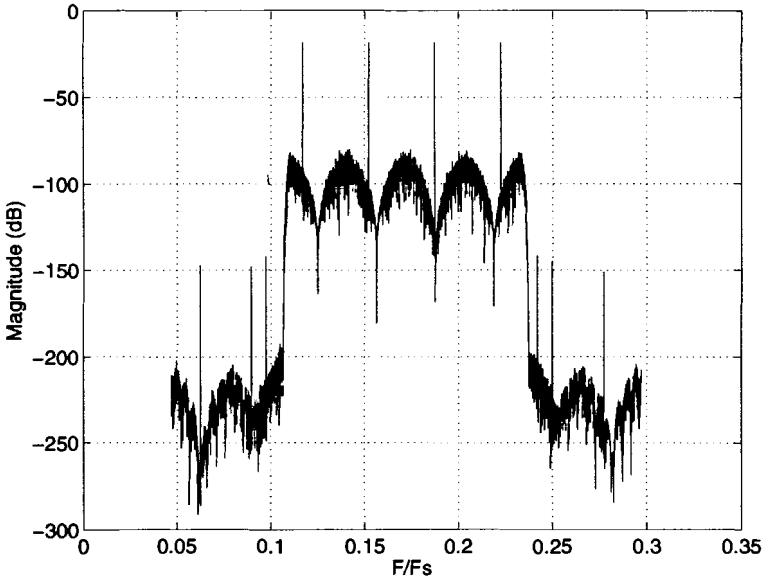
The results of a single-tone test are shown in Figure 4.10. The bands are quantized with $\Sigma\Delta$ ADCs using a second order loop are used in each channel. The narrow bandwidth high resolution region has been duplicated in channels 4 and 5 as shown in Figure 4.10(a), thus giving the $\Sigma\Delta$ recombination architecture twice the bandwidth of a single device. Thus only half of the output sampling bandwidth is unuseable, compared to the large portion of the output spectrum that usually goes to waste in a single $\Sigma\Delta$ ADC. Another advantage of this architecture is that the quantization noise that resides outside the band of interest, which is usually very high, has already been filtered out by the system so no additional filters are needed.

Multi-tone 4 band test

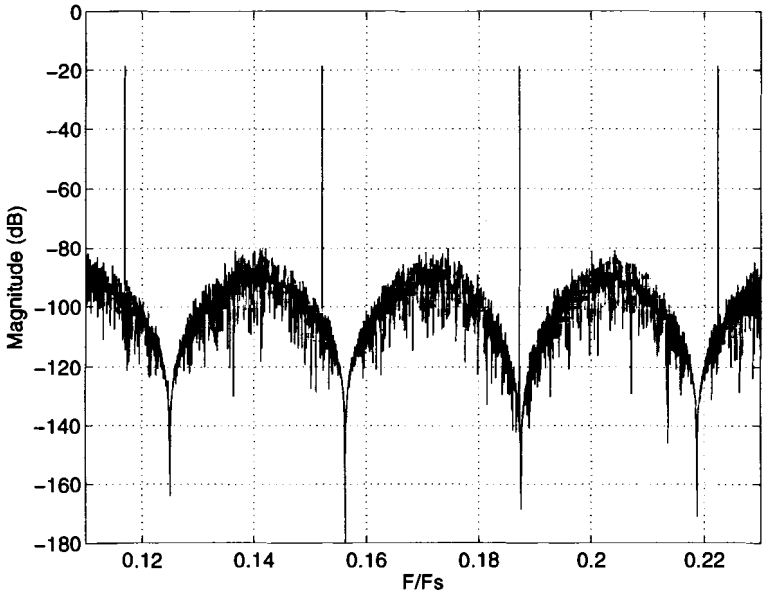
The system is designed to quantize wideband signals with the resolution of a $\Sigma\Delta$ converter, and the results of a wideband signal test appear in Figure 4.11. The signal is composed of four tones that span bands 4 through 7. Each band has again been shaped by the $\Sigma\Delta$ ADC, with each band taking advantage of the narrow bandwidth of the converter that has the highest resolution. Out-of-band signals are well attenuated so they do not interfere with the recombination that would take place in the following stages. These results show that the recombination of several quantized signals can be accomplished using this structure.

4.4 Conclusions

The architecture proposed in this thesis accomplishes several of the goals set forth in Chapter 1. The recombination filter bank is able to reliably recombine several quantized bands into one wideband signal. The filter bank design approximates a perfect reconstruction filter bank by using linear phase filters and relaxing the amplitude distortion



(a) Second order $\Sigma\Delta$ recombination



(b) Close up of Figure 4.11(a)

Figure 4.11: Four-tone test in bands 4 through 7

requirement. Simulations show a minimum amount of distortion across the entire band, including at the band edges. This amount of distortion is adjustable by using more coefficients in the filter design. The design presented in this chapter was able to realize a tolerable amount of distortion without using an exeptionally large number of coefficients.

The structure also allows the high resolution bandwidth of a $\Sigma\Delta$ ADC to be extended to cover a much wider range by using multiple devices at once. This allows the ADC to be used in the quantization of a wideband signal as opposed to just narrowband signals. The $\Sigma\Delta$ ADC can now be used in many more applications, which makes the oversampled device much more versatile. The cost of increased bandwidth is identical copies of the same device, which is already a simple and cost efficient device.

The flexibility of this architecture is one of its strongest points. All of the channels use identical hardware to operate on different bands. The design uses the same filters in every channel, which drastically reduces the number of coefficients to be stored in memory over that needed by other recombination filter banks that use different filters in each channel. All of the recombination blocks are identical in every stage with the exception of the phase shift correction factors. The feature that makes it most appealing for communications systems is that any set of bands may be recombined as long as the number of bands is a power of two. The other restriction is that each recombination stage must recombine adjacent pairs of bands. A bandwidth of any width centered at any one of the band centers may be reconstructed from its subband parts. All of the processing after the channel quantizer is done digitally, which also improves the reliablity of the structure.

CHAPTER 5

FREQUENCY-SELECTIVE ΣΔ MODULATOR

This chapter shows the new bandpass ΣΔ ADC that was designed and built as a prototype for the channel quantizers used in the structure described in this thesis [1]. The basics of ΣΔ quantization are included in a discussion on how the structure is implemented on the chip. The chip architecture is discussed, with emphasis on the design of the modulator that allows the ADC to produce complex samples of the bandpass signals. The performance of the combined system of the modulator and the converter is examined.

5.1 Project goals

The work shown in this thesis relies on a sampling module that can produce samples of the complex representation of a bandpass signal. The device described in earlier chapters performs this function using IQ modulation with lowpass ΣΔ ADCs in each channel. The ΣΔ ADC was chosen as the channel quantizer for its high resolution. The sampling module chooses a particular band of frequencies, modulates it down to baseband, and then quantizes the signal. The in-phase and quadrature samples created by this device can then be filtered and recombined in software in the manner described in earlier chapters to obtain high resolution conversion across a wide band of frequencies.

This chapter presents the design of one device that can produce the complex samples for each band of frequencies. A switched-capacitor technique allows the modulator at the beginning of the sampling module to be implemented in the front-end of the ΣΔ ADC in that module. Each module contains in-phase and quadrature channels, and each channel consists of a modulator and an ADC as discussed in Section 2.2.4. This one-chip solution to the IQ ΣΔ structure decreases the amount of hardware needed to quantize each band.

5.2 $\Sigma\Delta$ ADC basics

The block diagram of a first order $\Sigma\Delta$ ADC is shown in Figure 5.1(a). The structure consists of a summing node, an integrator, a one-bit ADC, and a one-bit DAC. For the purpose of system analysis, the ADC is modeled as a noise source that adds the quantization error $e[n]$ to the signal, which is simply the difference between the input of the ADC and the DAC output. The DAC is represented by a unity gain block, and the resulting structure appears in Figure 5.1(b) where the integrator is represented by a block that has z-transform

$$H_{int}(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{5.1}$$

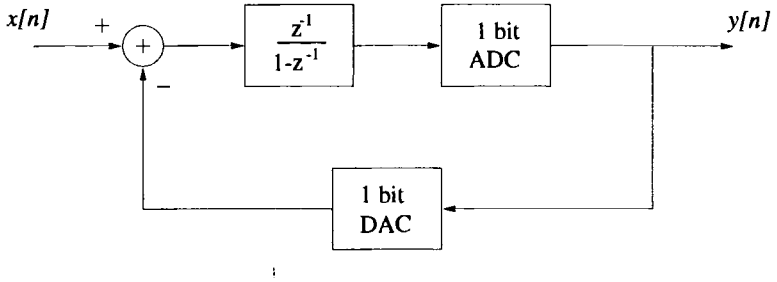
The z-transform analysis of the system shows that the signal $y[n]$ is composed of both $x[n]$ and $e[n]$

$$\begin{aligned} Y(z) &= z^{-1}X(z) + (1 - z^{-1})E(z) \\ &= H_s(z)X(z) + H_e(z)E(z) \end{aligned} \tag{5.2}$$

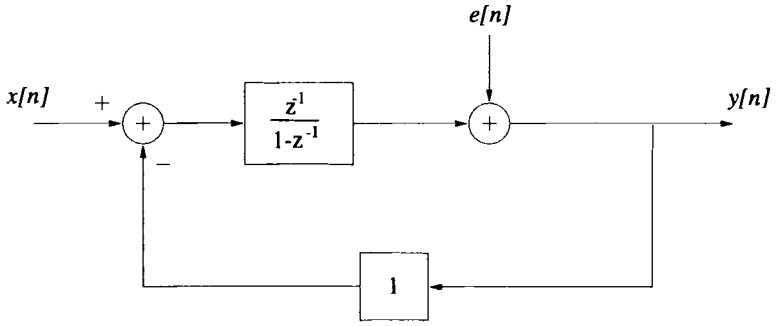
where $H_s(z)$ is the signal transfer function (STF) and $H_e(z)$ is the noise transfer function (NTF) of the system. These transfer functions are plotted in the frequency domain in Figure 5.2. The signal is passed through the system with just a sample delay while the quantization noise is attenuated at the origin and amplified with increasing frequency. The zero at $z = 1$ of $H_e(z)$ is what shapes the quantization noise in this manner. The result is a narrow region centered at the origin that has very high resolution [4].

Higher order converters may be constructed by increasing the loop order. A second order loop structure is shown in Figure 5.3. The transfer functions for the signal and error are found to be

$$H_s(z) = z^{-2}$$



(a) Actual block diagram



(b) Equivalent structure for analysis

Figure 5.1: Block diagram of a first order $\Sigma\Delta$ ADC

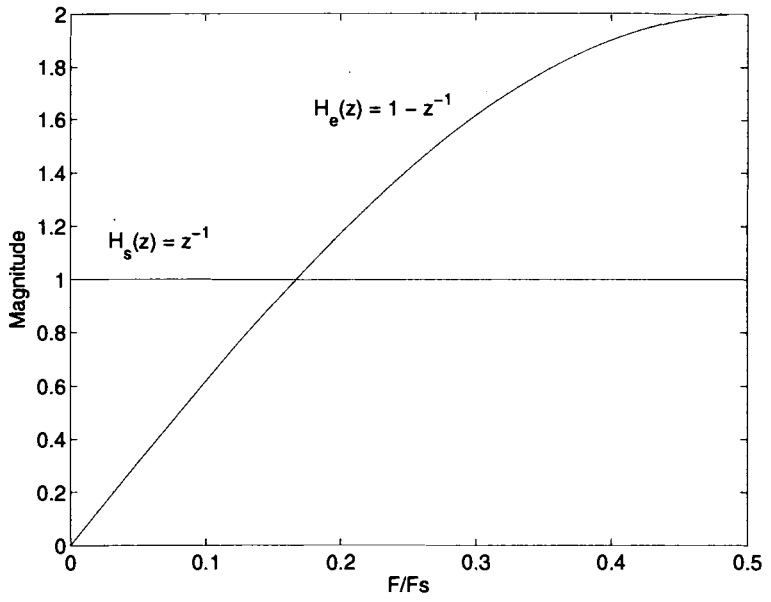


Figure 5.2: Frequency response associated with the transfer functions $H_s(Z)$ and $H_e(z)$ (first order loop)

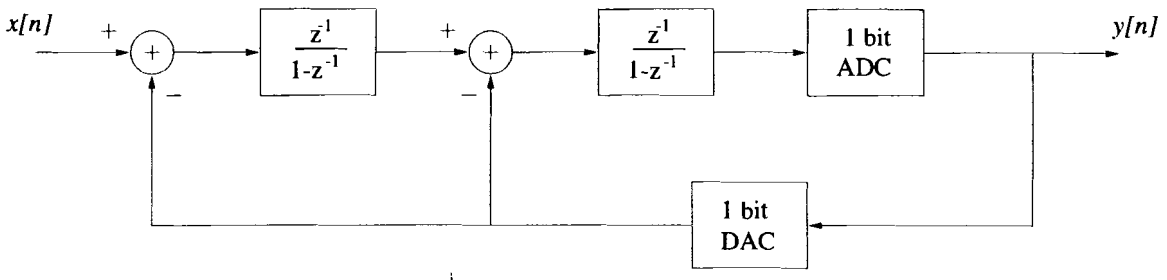


Figure 5.3: Block diagram of a second order $\Sigma\Delta$ ADC

$$\begin{aligned} H_e(z) &= (1 - z^{-1})^2 \\ &= 1 - 2z^{-1} + z^{-2} \end{aligned} \tag{5.3}$$

where the double zero at $z = 1$ shapes the quantization noise to a higher degree than the first order case, as is shown in Figure 5.4. $\Sigma\Delta$ ADC loops may be increased further in this manner, although they seldom are because the loop becomes unstable [10].

Another technique is used to implement $\Sigma\Delta$ ADCs with order greater than two. The multistage noise shaping (MASH) technique of $\Sigma\Delta$ quantization uses cascaded loops to increase the resolution of the converter [11, 12]. Figure 5.5 shows a cascaded architecture example. The second stage quantizes the error signal, $e_1[n]$, created by the first stage, leaving a smaller quantization error signal, $e_2[n]$, in the second stage. The bits are then digitally filtered to remove the error from the first stage. The first stage error is filtered by the STF and the second stage error is filtered by the NTF to yield

$$\begin{aligned} Y_{out}(z) &= z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z) \\ &= z^{-2}X(z) - (1 - z^{-1})^2 E_2(z) \end{aligned} \tag{5.4}$$

where the error signal $e_1[n]$ has been completely cancelled with a smaller error from the second stage. The NTF for the cascaded architecture is the square of the single first order loop NTF and the resulting error $e_2[n]$ is more random with respect to the signal.

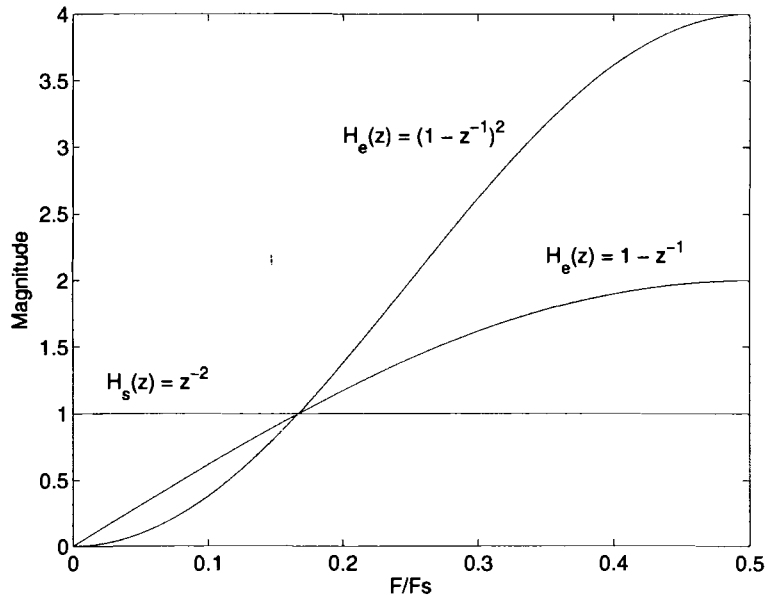


Figure 5.4: Transfer functions $h_s[n]$ and $h_e[n]$ (first and second order loops)

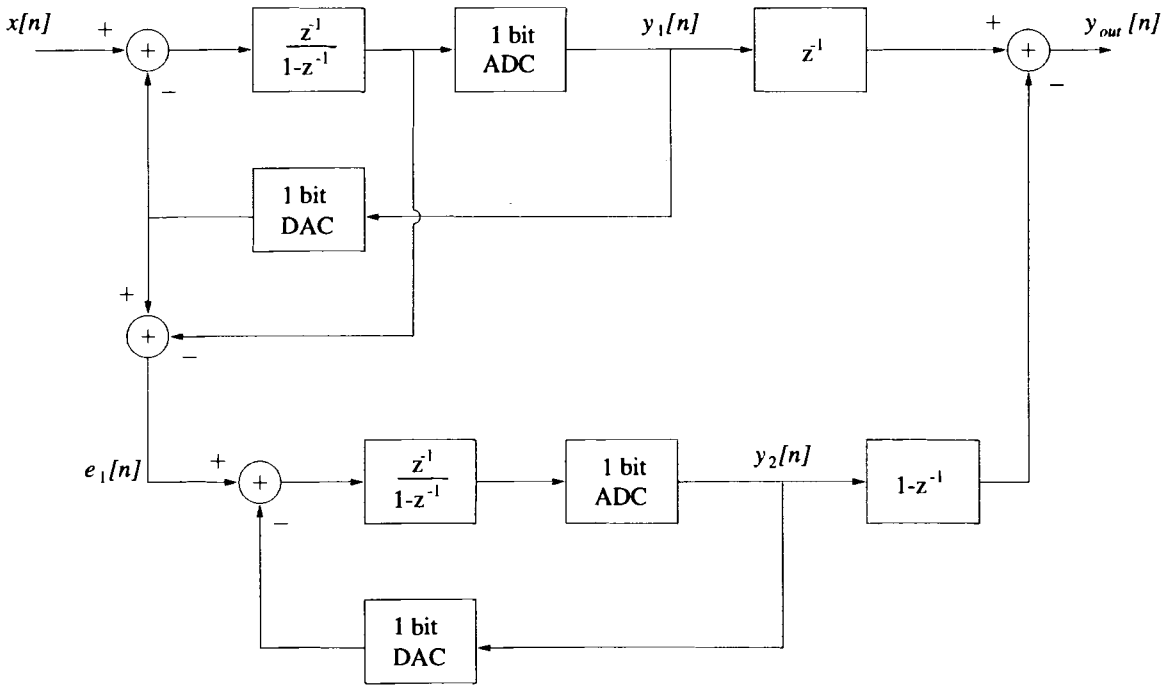


Figure 5.5: $\Sigma\Delta$ MASH architecture (second order)

ADC	$\Sigma\Delta$
topology	Fourth-order MASH
bandpass sampling method	IQ structure
OSR	32
bandwidth	$\frac{F_s}{32}$
quantizer size	1 bit
DAC size	1 bit
number of center frequencies	16
target ADC resolution	16.8 bits

Table 5.1: Device specifications for the ADC of [1]

A fourth order MASH architecture can be built by cascading two second order structures and filtering the output bits from each stage with the second order STF and NTF given by (5.3).

5.3 Chip specifications

For this device, complex samples of the bandpass representation of each subband signal are produced using in-phase and quadrature channels. The prototype built in [1] uses a fourth-order MASH architecture composed of cascaded second order loops in each channel. A fourth order $\Sigma\Delta$ topology was chosen to provide a high degree of resolution in each band. The theoretical bound on effective bits for a fourth-order $\Sigma\Delta$ modulator using one-bit quantizers is calculated to be 16.8 bits [13]. The pair of $\Sigma\Delta$ ADCs designed for this chip are implemented using switched-capacitor integrators. The converter uses a one-bit quantizer to quantize the input signals and a one-bit DAC in the feedback path of each loop. The device runs at an oversampling rate (OSR) of 32. On-chip digital filters provide the proper filtering at the output of each stage, although the raw output bits from each stage are also pinned out. The modulators are configured to select one of 16 bands across the first Nyquist band for quantization. These specifications are summarized in Table 5.1.

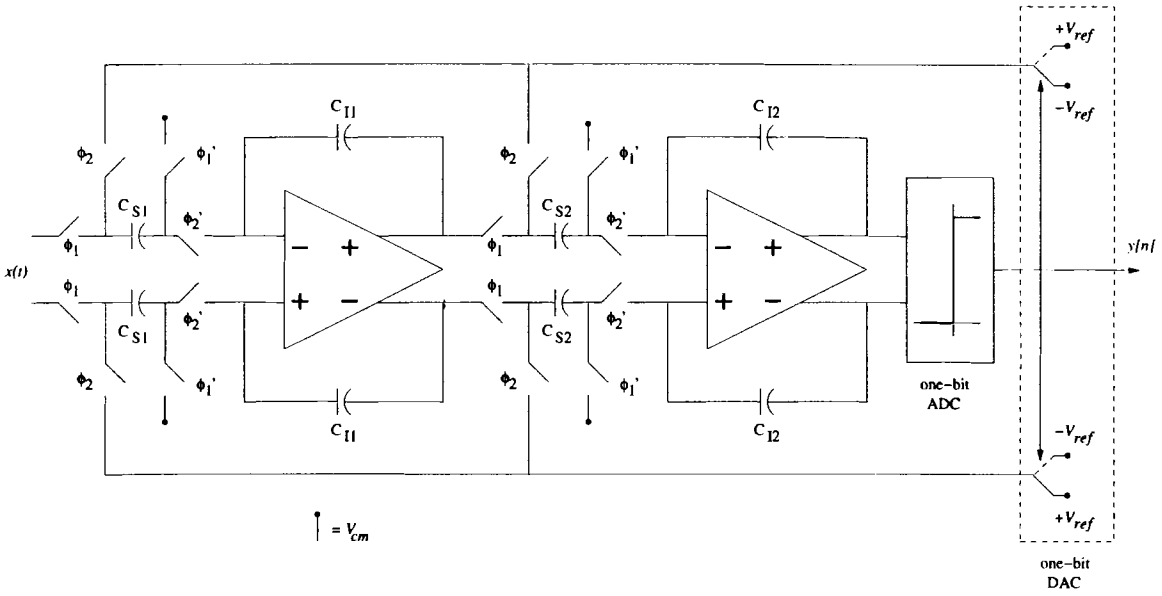


Figure 5.6: Second order $\Sigma\Delta$ modulator implementation

5.4 Major components

The two major parts of the circuit are the second order $\Sigma\Delta$ loop and modulator. The design of the $\Sigma\Delta$ loop is modeled after that shown in [10]. The modulator design is a new addition to the switched-capacitor $\Sigma\Delta$ circuit that was explained for the first time in [1].

5.4.1 Second-order $\Sigma\Delta$ loop

The fully differential second order $\Sigma\Delta$ loop used in this design is shown in Figure 5.6. The integrating feedback loop consists of two integrators, a one-bit ADC (a comparator), and a one-bit DAC (a switch). The integrators are implemented with a switched-capacitor circuit composed of two sets of capacitors and an operational amplifier (op-amp). The set of capacitors C_{S1} and C_{S2} that are switched sample the integrator input voltages and hold the charge to be integrated. The set of capacitors C_{I1} and C_{I2} store the charge for each integrator. An external clock supplied to the circuit is divided into two nonoverlapping phases, designated ϕ_1 and ϕ_2. During the sample phase

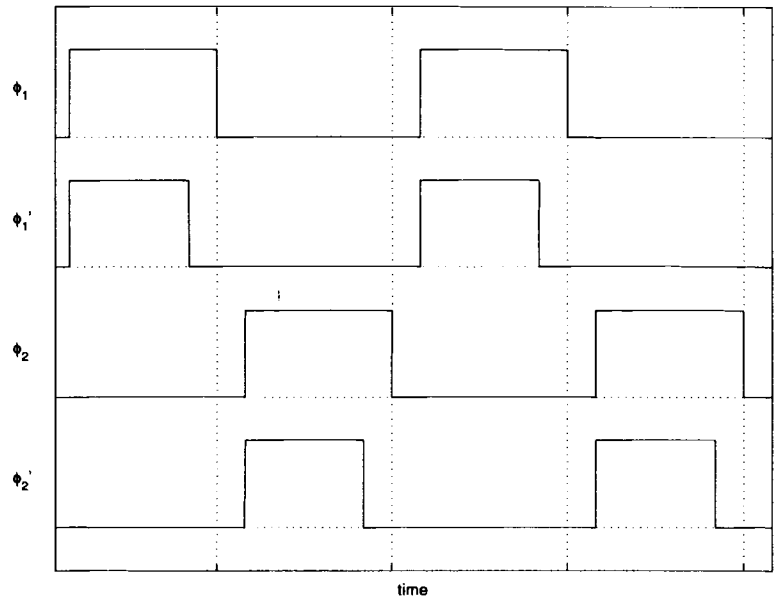


Figure 5.7: Clock phases for $\Sigma\Delta$ modulator of Figure 5.6

ϕ_1 is high (while ϕ_2 is low), and switches close that connect sampling capacitors C_{S1} to the input while another set of switches opens to isolate the sampling process from the charge already stored on the integration capacitors C_{I1}. The integration or summing phase occurs when ϕ_2 goes high (and ϕ_1 goes low), which opens switches between the input and C_{S1} and closes switches between C_{S1} and integrating capacitors C_{I1}. This allows the transfer of sampled charge to C_{I1} where it is stored for the next clock cycle. The second integrator consisting of capacitors C_{S2} and C_{I2} operates in the same manner for each clock phase.

The use of CMOS switches to transfer charge throughout the circuit can be problematic due to the issue of charge injection. This phenomenon occurs when the conducting channel inside a switch is shut down at the beginning of a new clock phase. The finite amount of charge inside the channel is forced out of the switch with different amounts going in either direction. The additional charge on the integrating capacitors can be a source of error for switched-capacitor $\Sigma\Delta$ ADCs. The differential topology of the circuit in Figure 5.6 removes this error to a first order because the combined

charge injected from switches on either side is a common-mode signal [10]. A technique called bottom plate sampling can significantly reduce the amount of signal-dependent charge injection that takes place in the integrator [10, 14]. The switch that controls the bottom-plate of C_{S1} (the plate not connected to the input signal) is always opened slightly before the switch on the top plate. The opening of the bottom plate switch leaves the bottom plate of the capacitor floating while the charge is effectively trapped on C_{S1}. The signal dependent charge that would be injected upon the closing of the top plate switch cannot be forced onto C_{S1} because there is no closed path for current to flow through. Additional clock phases ϕ_1' and ϕ_2' are created to clock the bottom plate switches, where ϕ_1' goes low slightly before ϕ_1 and ϕ_2' goes low slightly before ϕ_2. The timing diagram that shows the different clock phases relative to one another appears in Figure 5.7.

The rest of this circuit consists of the comparator and the DAC switches. The comparator creates the digital output based on the polarity of the output of the second integrator. The DAC switches are controlled by the comparator output, and they feedback the appropriate voltage ($+V_{ref}$ or $-V_{ref}$) to either side of the integrators. The closing of the switches clocked by ϕ_2 effectively supplies the difference between the sampled voltages on capacitors C_{S1} and C_{S2} and the DAC output to the input of each integrator. To zero a signal in the circuit, both nodes of the differential signal are tied to a common mode reference V_{cm} (shown in Figure 5.6) which is the middle of the voltage supply rails.

5.4.2 IQ modulator

This device uses real and imaginary channels in order to produce complex samples as discussed in Section 2.2. The cosine and sine wave signals that modulate the input signal for frequency translation can be generated by modulating the charge sampled from the input voltage by the first integrator in each loop. In order to modulate the input

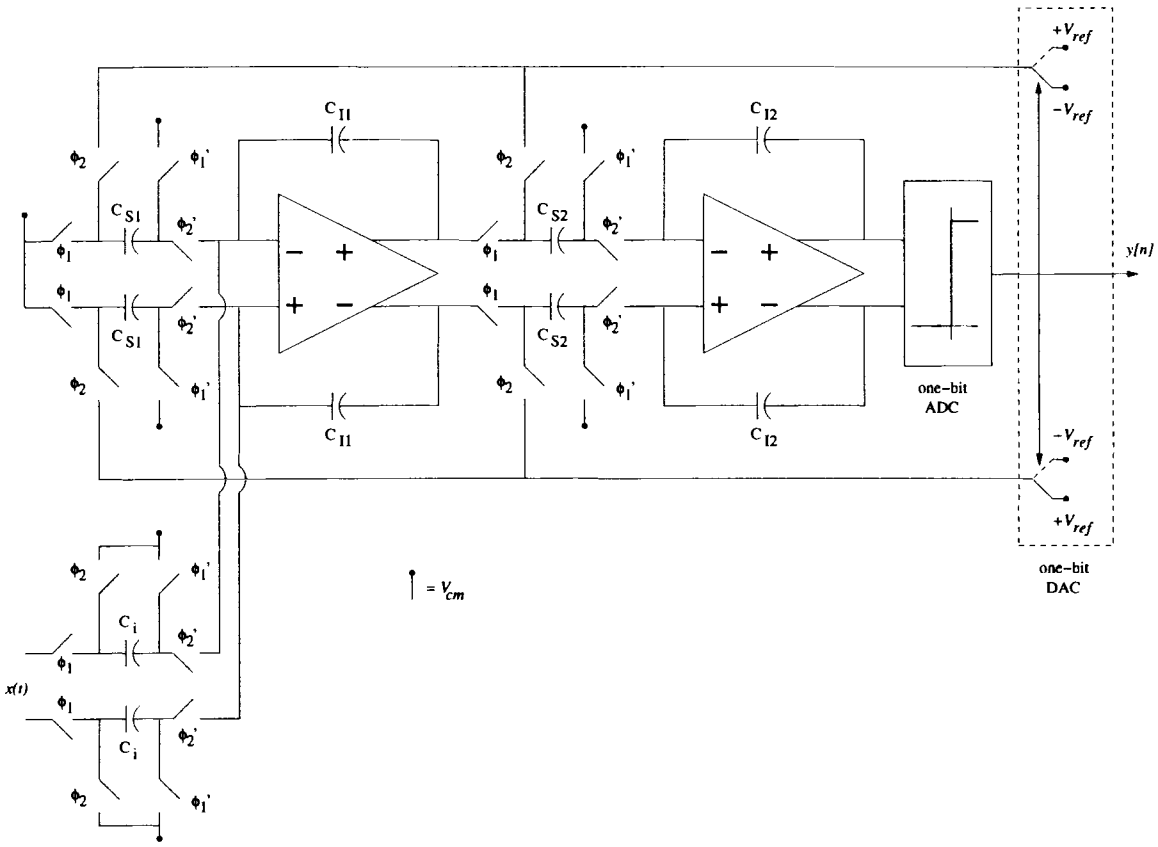


Figure 5.8: Second order ΣΔ loop with modulator sampling capacitors

signal with a cosine wave, the charge is sampled by several different relative capacitance values, which are chosen from one full period of a cosine wave. Storing the charge on each capacitor in the correct sequence effectively modulates the charge with a cosine or sine wave. The new $\Sigma\Delta$ loop using modulation capacitors C_i is shown in Figure 5.8. The capacitors that sample the feedback voltages generated by the DAC are the same capacitors C_{S1} that appear in Figure 5.6 in order to set the gain of the integrator. The number of center frequencies must match the OSR in order to select bands centered at multiples of F_s/OSR. For an OSR of 32, there are 32 capacitance values in the full cycle of the cosine wave. The values used for capacitor C_i are generated from the equation

$$C_i = C_U \cos\left(\frac{2\pi(i+\frac{1}{2})}{\text{OSR}}\right) \qquad i = 0, 1, 2, \ldots \text{OSR} - 1 \tag{5.5}$$

where C_U is the unit capacitor that all values are scaled by to maintain the proper gain in the integrator, and the offset of $\frac{1}{2}$ has been included so that the in-phase and quadrature channels can use the same set of capacitors. By replacing cos() with sin() in (5.5) the same values are generated, although in a different sequence. The offset eliminates the problem of overlap in the sequences for cosine and sine waves, allowing both waveforms to be generated from the same set of capacitors. The relative capacitance values $\frac{C_i}{C_U}$ generated for an OSR of 32 are shown in Figure 5.9.

If all 32 capacitor values are used in sequence, the period of the modulating wave will be 32 clock cycles, as it takes that long to reach the first value used. By comparing the period of the clock to that of the waveform consisting of the sequence of capacitance values, the frequency of modulation is found to be

$$F_m = \frac{F_s}{32}. \tag{5.6}$$

The input signal is effectively modulated with a cosine wave at a frequency of $F_s/32$. Using the sine wave capacitor value sequence in the opposite channel and combining

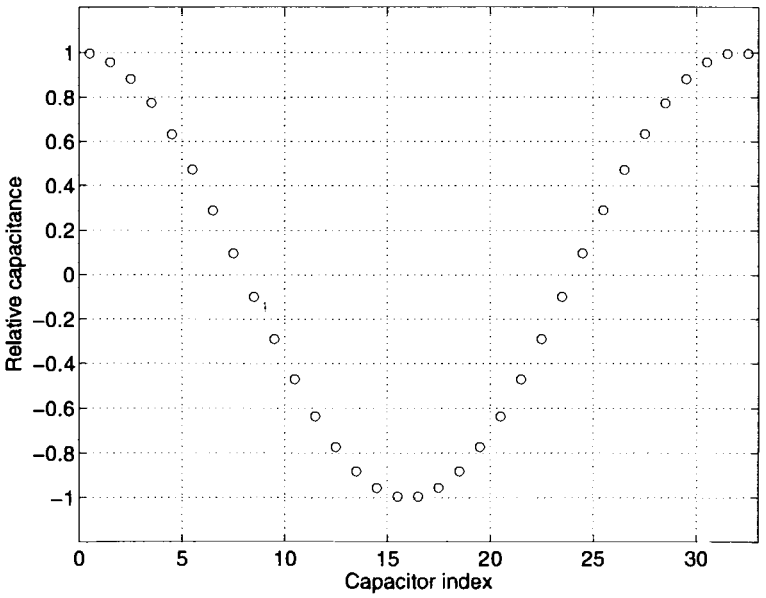


Figure 5.9: Relative modulator capacitance values for OSR of 32

the real and imaginary outputs yields a signal that is translated in frequency towards the origin by F_m. This modulation sequence using all capacitance values enables a lowpass $\Sigma\Delta$ ADC to operate on the $k = 1$ band as explained in Section 2.3.

Multiples of this frequency can be generated by using the same capacitor values in a different sequence. For example, using every third capacitor value still takes 32 clock cycles to get back to the first capacitor value as shown in Figure 5.10. At the end of 32 clock cycles the values have cycled through three periods of a cosine wave. The corresponding frequency of modulation is found as in (5.5)

$$F_m = \frac{3F_s}{32} \tag{5.7}$$

which translates the signal spectrum so the $k = 3$ band can be processed by the lowpass ADC. Other modulation frequencies can be achieved in the same manner. For modulation by $\frac{nF_s}{32}$, every nth capacitance value is used. In order to operate on the $k = 0$ band, the first capacitor is used to collect every sample.

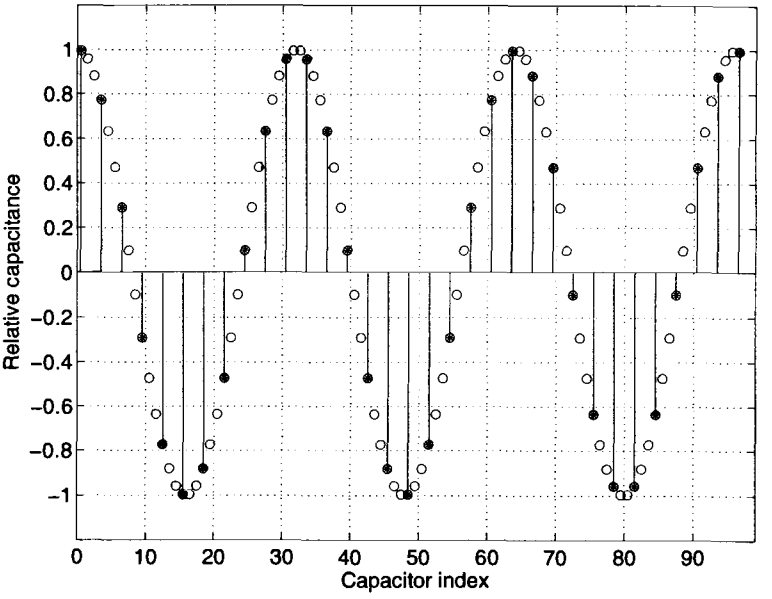


Figure 5.10: Relative modulator capacitance sequence for $F_m = \frac{3F_s}{32}$

capacitor	value (fF)	subunit size (fF)	number of subunits
C_0	199.04	19.90	10
C_1	191.39	19.13	10
C_2	176.38	19.59	9
C_3	154.60	19.32	8
C_4	126.88	21.14	6
C_5	94.28	18.85	5
C_6	58.06	19.36	3
C_7	19.60	19.55	1

Table 5.2: Modulator capacitor and subunit values

Inspection of the values in Figure 5.9 shows that the first 8 values can be used to generate the entire sequence of capacitances. The other 24 values are created by reversing the order and polarity of the first set of 8 capacitors in such a manner that forms a cosine wave. This saves a lot of area in the layout process, as capacitors consume much more space than the circuits that will replace them. Small valued capacitors built from plates constructed on two different metal layers make up subunits that are pieced together to form the larger valued capacitors. The capacitor values and subunit values are given in Table 5.2, where the values are all chosen relative to $C_U = 200$ fF for this circuit, which is the value used for capacitors C_{S1} to sample the feedback voltages in Figure 5.8.

The modulator is implemented using two matched sets of eight sinusiodally weighted capacitors, one set for each side in the differential topology. A barrel counter that counts in increments of 0 to 15 using modulo 32 arithmetic is used to find the position in the sequence for every clock cycle, and logic circuits then select the particular capacitance that each channel uses to sample the signal.

The block diagram of the contents of the chip appear in Figure 5.11. The modulator takes the input signal and feeds the modulated in-phase and quadrature signals to the fourth order lowpass MASH architecture $\Sigma\Delta$ ADCs in each channel. The digital filters, consisting of D flip-flops that act as hold registers, and basic logic gates, create the output words $w_I[n]$ and $w_Q[n]$ from the output bits from each stage.

5.5 Chip layout

This device was designed in the Microelectronics Lab in the Electrical and Computer Engineering Department at the University of Maine. It was fabricated by MOSIS using a CMOS process technology from AMI Semiconductor. The AMIS C5N process is a single well, double poly, triple metal process with a minimum gate length of 0.6 μm designed on a grid using 0.15 μm spacing. The device operates using a 5 V supply

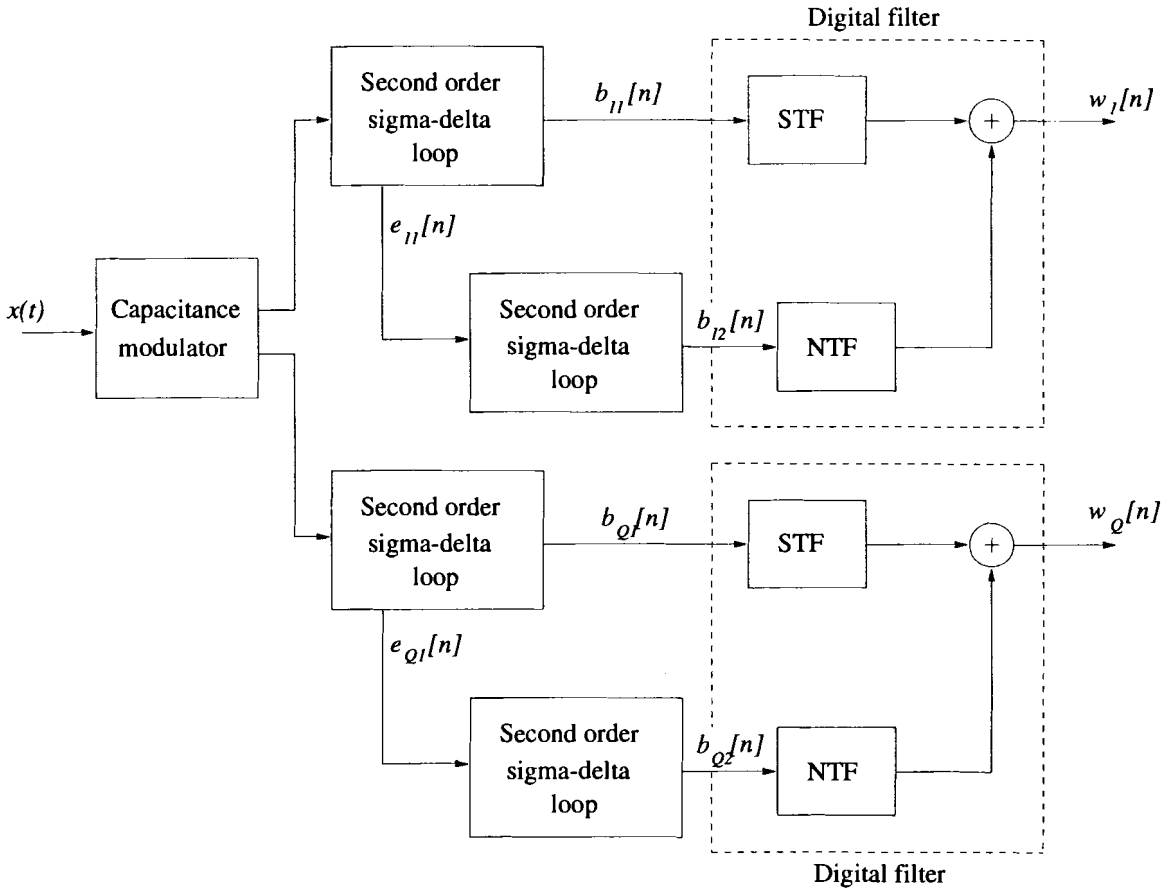


Figure 5.11: Block diagram of frequency selective $\Sigma\Delta$ ADC

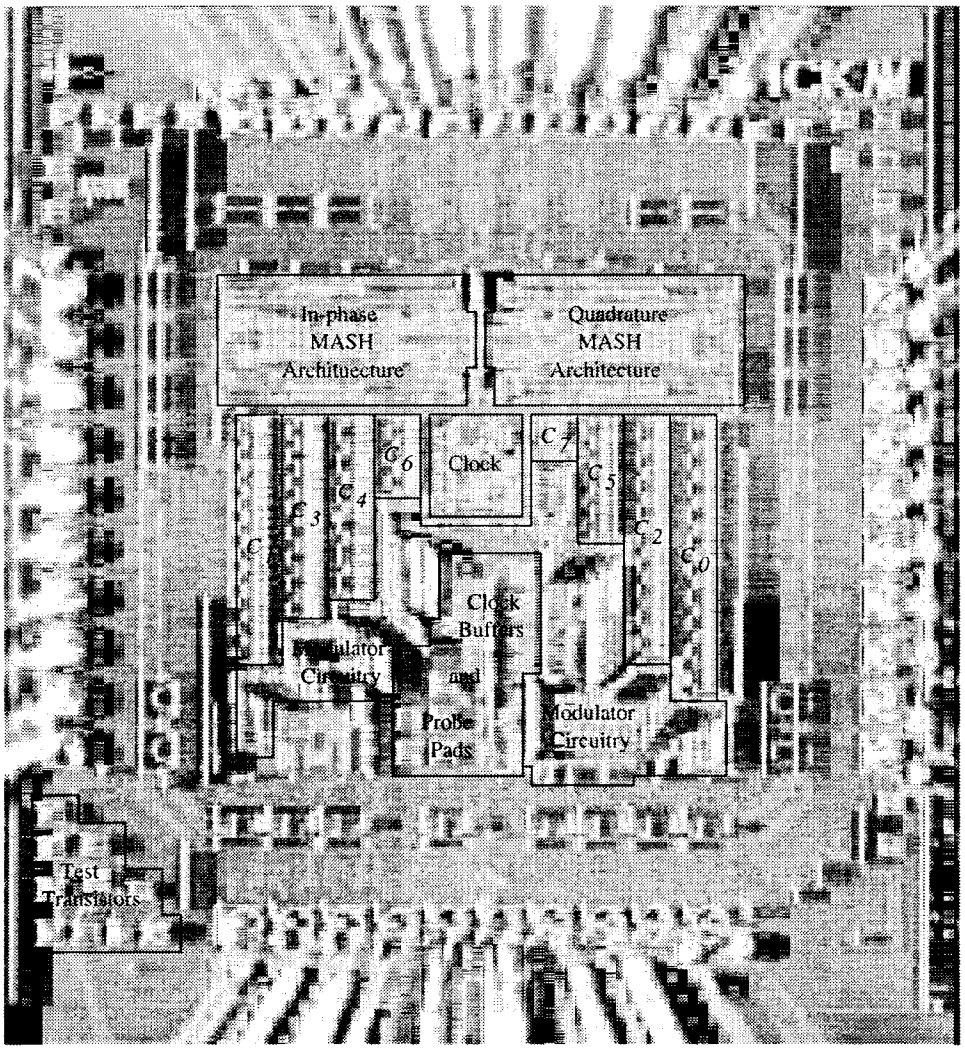


Figure 5.12: Digital image of packaged die

clock frequency	4.096 MHz
clock amplitude	0.85 V
signal amplitude	0.12 V
V_{cm}	2.5 V
V_{ref+}	V_{cm} + 0.35 V
V_{ref-}	V_{cm} − 0.35 V

Table 5.3: Test conditions for performance evaluation of the fabricated device

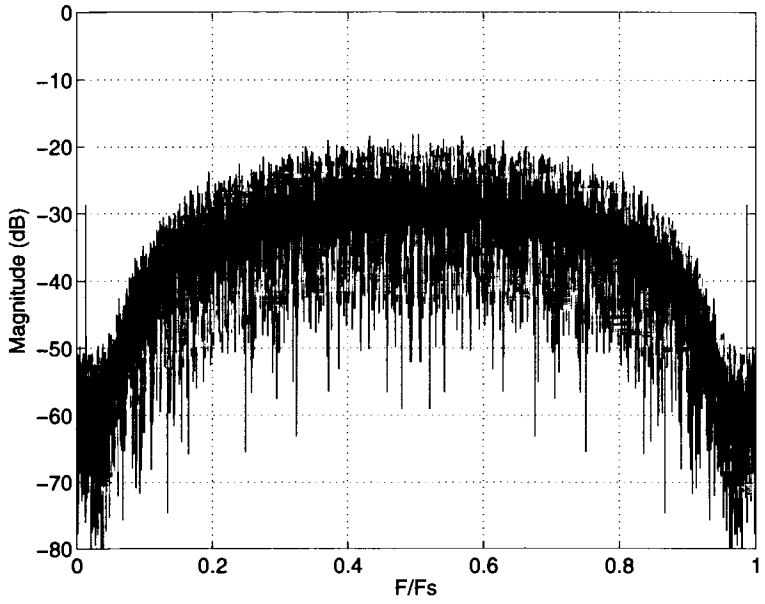
rail. The total die size is 1.5 mm × 1.5 mm, and the chip is packaged in a 40 pin DIP. Figure 5.12 shows a photograph of the fabricated chip including the floorplan of the major components. The detailed report of the design, layout, and testing of this device may be found in [1].

5.6 Performance

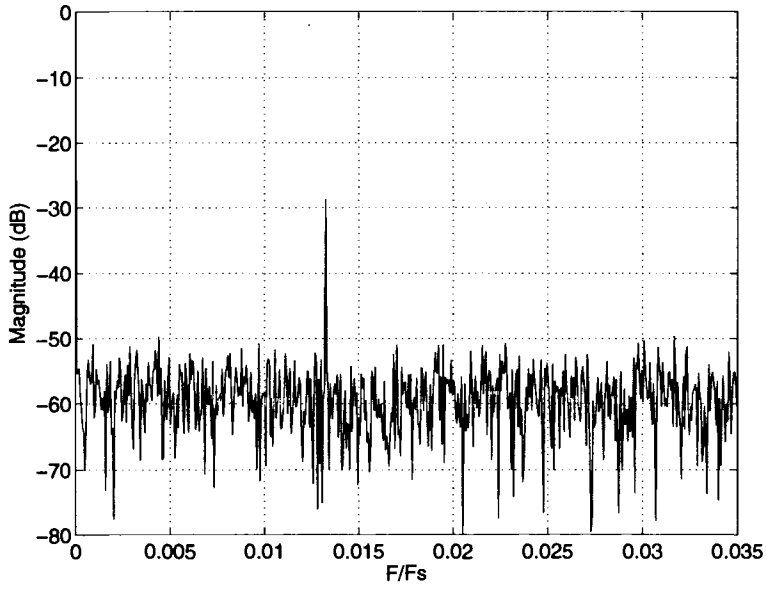
The performance of the fabricated chip was evaluated using an evaluation board designed specifically for this chip. The circuit includes switches that are set to select the frequency of operation, drivers for the output bits, and reference voltage circuits. The printed circuit board was fabricated by AP Circuits and assembled in the Communications Lab in the Electrical and Computer Engineering Department at the University of Maine. The instruments on the test bench in the lab were used to drive the circuit and collect measurements. All of the tests described in this section were run under the same conditions, which are summarized in Table 5.3. The signal amplitude is small due to the number of integrators that process the signal. The stored charge builds up quickly, and signals must be small to avoid clipping inside the integrators which leads to errors in the output code.

5.6.1 Baseband test

The first test was conducted on the $\Sigma\Delta$ ADC with the modulator disabled in order to evaluate the performance of the lowpass ADC that processes each band. The



(a) Full output spectrum



(b) Magnification of output spectrum near baseband

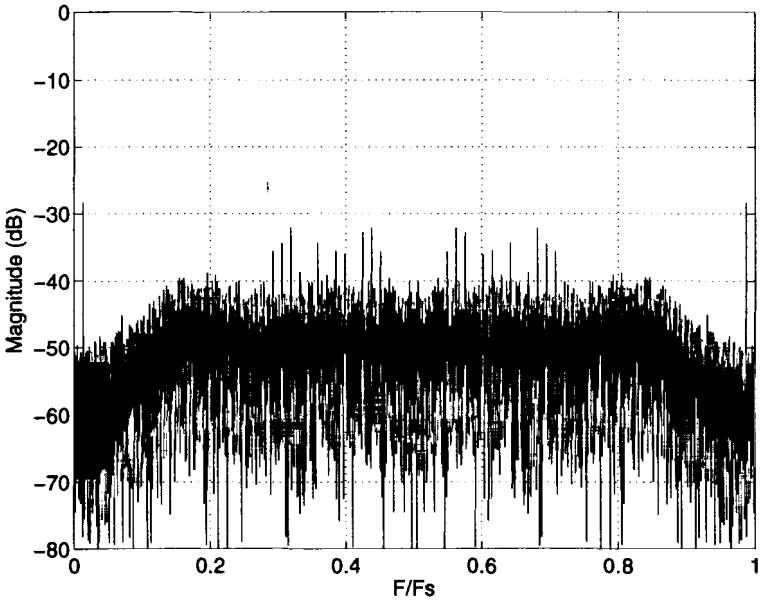
Figure 5.13: Baseband test results (16 ksamples)

$k = 0$ band was selected for operation, which causes the modulator to use only the largest capacitor, C_0, to sample the input signal. In this mode, the device simply acts as a lowpass $\Sigma\Delta$ ADC. The only outputs that are valid are those from the in-phase side, because the converter is processing a real signal at all points in the system. The output spectrum is symmetric about $f = \frac{1}{2}$ since the output is not complex valued. The input signal contained energy at a frequency of 54.25 kHz ($f = 0.0132$), which lies within the bandwidth of the lowpass $\Sigma\Delta$ ADC, and $2^{14} = 16384$ samples were collected.

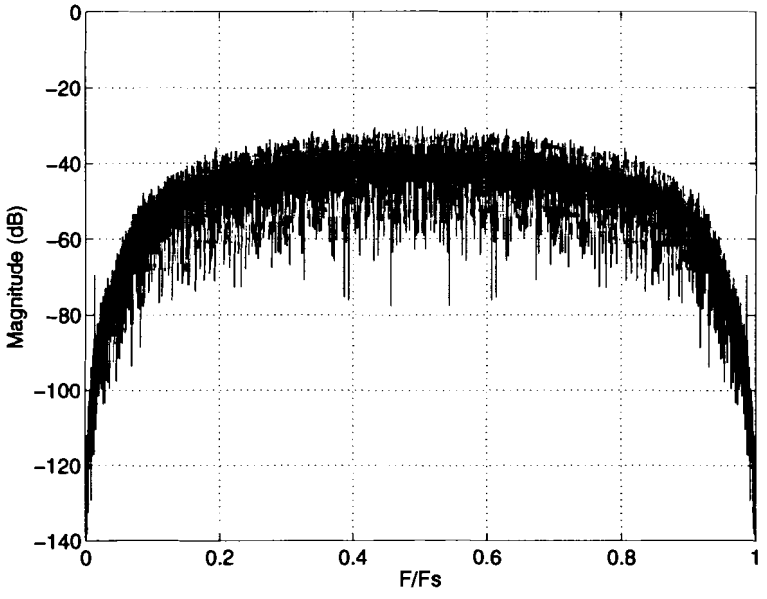
The output spectrum of the filtered data collected from both stages of the MASH architecture is shown in Figure 5.13. The fourth order noise shaping characteristic can be seen towards the middle of the band in Figure 5.13(a) where the quantization noise has a high arching shape. Unfortunately this noise shaping does not extend to the edges of the spectrum, where it is desireable to have very low quantization noise. Instead, the noise shaping characteristic levels off with decreasing frequency. Figure 5.13(b) shows that a constant noise level is reached at very low frequencies. With limitations on the size of the input signal, the poor resolution of the converter near baseband is exaggerated.

This problem can be traced to the first stage of the fourth order topology. The output spectrum of the bitstream produced by the first stage appears in Figure 5.14(a), while the bitstream from the second stage that has been filtered by the second order NTF of (5.3) is shown in Figure 5.14(b). The noise shaping of the first stage shows the same behavior as the combined output from both stages. It is apparent from the inspection of Figure 5.14 that when the two signals are added together, the first stage dominates at low frequencies while the second stage characteristic emerges with increasing frequency.

The poor noise shaping at lower frequencies may be attributed to a leakage factor, γ, in the integrators. The behavior displayed by the chip closely resembles that shown by leaky integrators caused by finite op-amp gain [13, 15]. The transfer function



(a) First stage output spectrum



(b) Filtered second stage output spectrum

Figure 5.14: Baseband test results from each stage (16 ksamples)

of the integrators used to build the $\Sigma\Delta$ loops given in (5.1) is changed to

$$H_{int}(z) = \frac{z^{-1}}{1 - \gamma z^{-1}} \tag{5.8}$$

which alters the STF and NTF for the loop. The NTF is now given by

$$H_e(z) = \frac{1 - \gamma z^{-1}}{1 + (1 - \gamma) z^{-1}} \tag{5.9}$$

where the zero at $z = 1$ that previously shaped the noise away from the origin of the frequency domain has been moved. In the switched-capacitor implementation, capacitor mismatches can also contribute to integrator leakage, and these problems become more severe if a MASH architecture is employed [13].

5.6.2 Adjacent band tests

The next test involves the combination of the modulator with both in-phase and quadrature quantizers in order to test the functionality of the entire device. Two adjacent bands, the $k = 4$ and $k = 5$ bands were selected for operation. In this mode, the modulator cycles through capacitance values to modulate the proper bands down to baseband. One test signal was used which contained energy at a frequency of 532.125 kHz ($f = 0.1299$) in the $k = 4$ band. This same signal is processed by the system operating on both bands, in order to examine how signals in adjacent bands are processed. For this test, $2^{15} = 32768$ samples were taken.

The output spectrum of the combined real and imaginary bits for the first part of the test (operation on the $k = 4$ band) appears in Figure 5.15. The noise shaping characteristic seen in the previous test appears again for this case. The output is not symmetric due to the complex output bits. There is one tone in the output bandwidth of the lowpass $\Sigma\Delta$ ADC, which is the modulated input signal. The tone apppears at

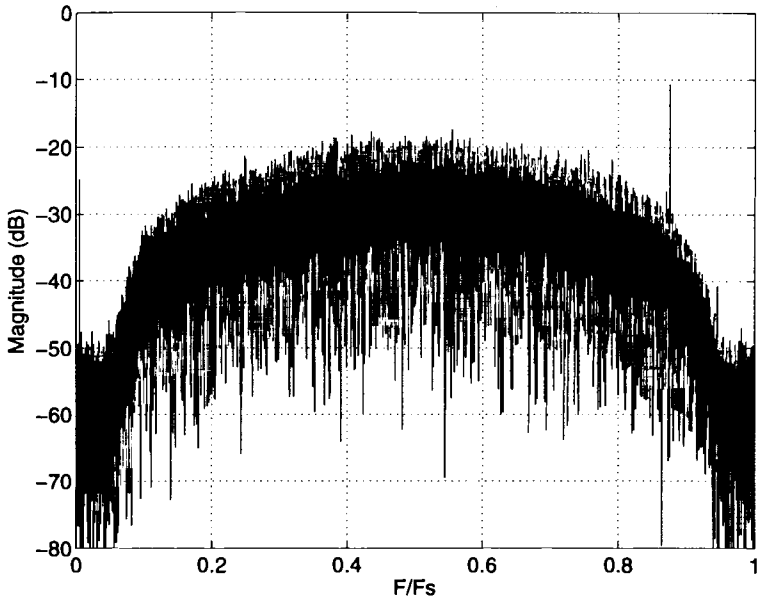


Figure 5.15: Test results from $k = 4$ band (32 ksamples)

the correct frequency for having been translated in frequency by $\frac{4F_s}{32} = \frac{F_s}{8}$ ($f = 0.125$). This would indicate that the modulator is operating correctly.

The second part of the test (operation on the $k = 5$ band) yields similar results, which are shown in Figure 5.16. Here the same test signal has been used, and the device is operating on the adjacent band. Once again the output tone appears on the correct frequency after modulation, this time outside of the bandwidth of the quantizer. This shows that the device can indeed select a specific band of frequencies to quantize, proving that such a device can be constructed for the architecture proposed in this thesis.

5.7 Conclusions

This chapter has given a brief overview of $\Sigma\Delta$ quantization basics and the circuit fabricated in [1] in support of this thesis. The testing outlined in the previous section shows that the proposed scheme of implementing the in-phase and quadrature modulators in the switched capacitor structure does have merit, as the proper bands of frequencies

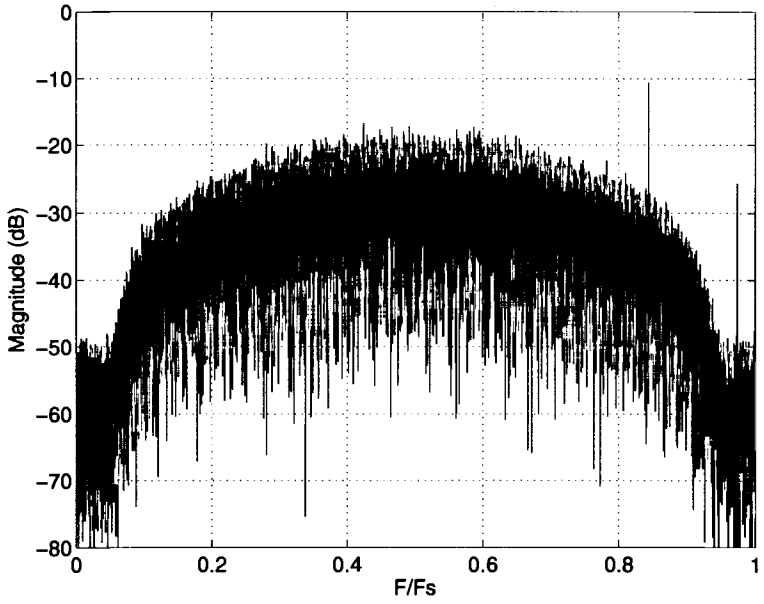


Figure 5.16: Test results from $k = 5$ band (32 ksamples)

were selected for lowpass $\Sigma\Delta$ modulation. The modulator designed in this thesis can be used in other bandpass ADC architectures to create complex samples.

The ability of the $\Sigma\Delta$ ADC designed in [1] to quantize the bandpass signals with a high degree of resolution leaves something to be desired. Fabrication tolerances on the capacitors in this process are suspected to be the main reason that the resolution of this device is so low. In order to quantize a signal with 16-bit resolution, the capacitors should be matched with the same accuracy, which is approximately one part in 65000. The capacitors in this process are manufactured with a tolerance that is much larger than this requirement, and as such are not matched to a 16-bit level. Capacitors built using different metal layers have much lower tolerances, but also take much more space on the chip. Another attempt at this should should use a larger die size in order to fit bigger capacitors, or a simpler ADC rather than a fourth-order design in order to reduce the number of capacitors.

The printed circuit board designed for evaluating the performance of the frequency selective $\Sigma\Delta$ ADC appears to have performed well. Data was collected using the board

that indicates the device does produce complex samples of signals residing in different bands of the frequency spectrum. The only improvement to be made is to manufacture a board that can support the operation of two or more frequency-selective $\Sigma\Delta$ ADC chips simultaneously, as the current board can only support one chip. This will allow the collection of coherent samples in each band, and the recombination filter bank can then be evaluated for samples taken by a real device.

CHAPTER 6

CONCLUSIONS

This chapter draws conclusions made concerning the work done in this thesis. Both the proposed architecture and the device examined in Chapter 5 are discussed, and ideas on future work in this area are given.

6.1 Proposed architecture

This thesis has shown that a recombination filter bank can be designed that can recombine several quantized bands to yield an output with wider bandwidth than a single device. The system approximates the perfect recombination of the quantized bands with a minimum number of filter designs. The filter designs are not complex and use a relatively small number of coefficients. The architecture is flexible with regard to the location and width of the recombined signal bands, which makes it ideal for implementing several different methods of reception in the same system. The only limitation on this system is that the number of recombined bands must be a power of two. All channels consist of the same hardware, and identical recombination blocks are used in each stage. This system can be implemented in software without having to store a large number of coefficients or instructions in memory.

One possible area for future work is the design of a similar system that uses a different type of ADC to quantize the signals in each band. A quantizer with a wider output bandwidth could be used to decrease the number of channels needed to quantize a given bandwidth. The filtering scheme is another topic that may be improved upon. An architecture composed of filters that allow maximal decimation in each channel makes for a much more efficient system, whereas the signal only occupies half of the output bandwidth at each stage in the current realization. Some form of simple perfect reconstruction bank may allow for a maximally decimated filter bank.

6.2 Channel quantization device

The device constructed for the sampling module described in Chapter 5 is able to produce samples of the complex representation of different bandpass signals. The modulator implemented in the front end of the $\Sigma\Delta$ ADCs in each channel translates the proper band of frequencies down to baseband. The fourth order $\Sigma\Delta$ ADC in each channel does not provide the resolution expected near baseband, although the noise shaping characteristic at higher frequencies appears to fit the shaping predicted by theory.

The fourth order MASH architecture $\Sigma\Delta$ ADC is a complex structure. The cascaded architecture requires precise matching between stages that contradicts the use of simple components in these quantizers [10, 16]. The use of lower order loops outside of a MASH architecture may yield higher resolution in the device. A process with tighter manufacturing tolerance on capacitors will also improve resolution. Once a device can be constructed that employs both a working modulator and a $\Sigma\Delta$ converter with high resolution, the use of cascaded loops may be investigated. As stated in the previous chapter, the testing of the sampling module should include running two devices simultaneously to collect samples from adjacent bands. Another possible improvement to the device is the use of Hadamard modulation [17], which only uses ± 1 to translate the signals in frequency. This would eliminate the need for high precision capacitors, which are difficult to construct in VLSI technology.

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